XVME-400 / XVME-401 / XVME-490 / XVME-491
4-Channel Serial I/O Modules

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.

Tel: (248) 295-0885
Fax: (248) 624-9234
Email: xembeddedsales@acromag.com

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xycom
Technical Publications Department
750 North Maple Road
Saline, MI 48176–1292

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Chapter 1

INTRODUCTION

1.1 OVERVIEW

The XVME-400, XVME-401, XVME-490, and XVME-491 are Quad Serial I/O VMEbus-compatible modules which provide a VME system with four serial communications channels. The XVME-400 and XVME-401 are single-high, while the XVME-490 and XVME-491 are double-high. The XVME-400 and XVME-401 access the I/O through the JKl and JK2 connectors on the module front panel, whereas the XVME-490 and XVME-491 route their I/O to the VMEbus P2 connector.

The XVME-400 and XVME-490 each provide four RS-232C serial ports, while the XVME-401 and XVME-491 each provide four RS-485/422A serial ports. (Differences among these modules are further detailed in Chapter 2, notably in Tables 2-1 and 2-2.)

Each module contains two 8530 Serial Communication Controller (SCC) chips, designated SCC #l and SCC #2. The two SCC serial chips provide a variety of communication modes, including asynchronous, byte-synchronous, and bit-oriented protocols. Each channel is independently programmable and has its own baud rate generator.

The VMEbus interface directly maps the SCC chips into the short I/O address space, starting on a jumper-selected 1 Kbyte boundary. The modules can also be jumpered to generate an interrupt on any of the seven VMEbus interrupt levels. The two SCC chips can generate a total of 16 different interrupt vectors.

Some features of the XVME-400/40l/490/491 modules include:

- Four independent full-duplex serial I/O channels
- RS-232C or RS485/422A operation
- Serial channels independently configurable for asynchronous, monosynchronous, bisynchronous, or HDLC/SDLC message formats
- Independent baud rate generators for each serial channel
- Modem control
- Receivers are quadruply buffered, transmitters double buffered
- Complete VMEbus interrupter, jumper-selectable to any interrupt level
- Programmable IACK vector, with vector alteration based on source of interrupt
- Line drivers for each channel are tri-stateable (controlled by software) to allow multidrop operation (XVME-401 and XVME-491 only)

1.2 MANUAL STRUCTURE

The chapters in this manual are structured as follows:

Chapter One - A general description of the XVME-400/401/490/491 modules, including complete functional and environmental specifications, VMEbus compliance information, and block diagrams.

Chanter Two - Module installation information, covering module-specific system requirements, jumpers, and connector pinouts.

Chapter Three - Details covering functional addressing, interrupt enabling, and programming considerations and requirements.

Appendix A - VMEbus connector and pin descriptions.

Appendix B - Quick reference guide with jumper configurations.

Appendix C - Block diagrams, assembly drawings, and schematics.

NOTE

This manual (XYCOM part # 74400-002) is part of a manual kit (XYCOM part # 74400-001) that is being shipped with the XVME-400/401/490/491 Modules. The kit also contains an 8530 Manual' (referenced as XYCOM part # 74400-003).

This manual discusses module base addressing, register access offsets, interrupt control, handshake control, and operational mode/programming constraints. To better understand these topics, is it recommended that you first read the 8530 Manual.

[1] Z8030/Z8530 SCC Serial Communications Controller Technical Manual, Zilog, January, 1983.

1.3 MODULE OPERATIONAL DESCRIPTION

Figure 1-1 shows an operational block diagram of the XVME-400 and XVME-490, and Figure 1-2 shows the block diagram for the XVME-401 and XVME-491.

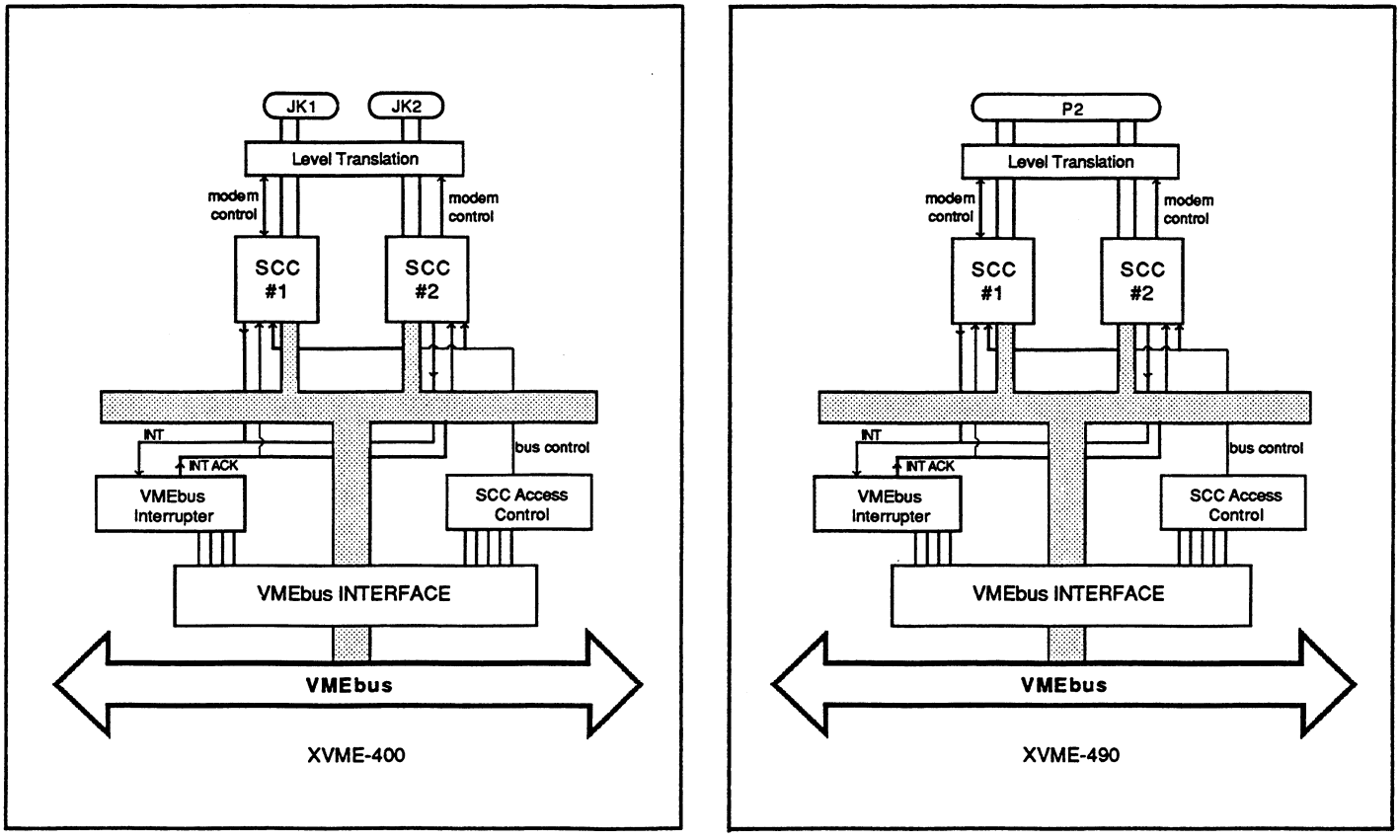


Figure 1-1. XVME-400 and XVME-490 Operational Block Diagrams

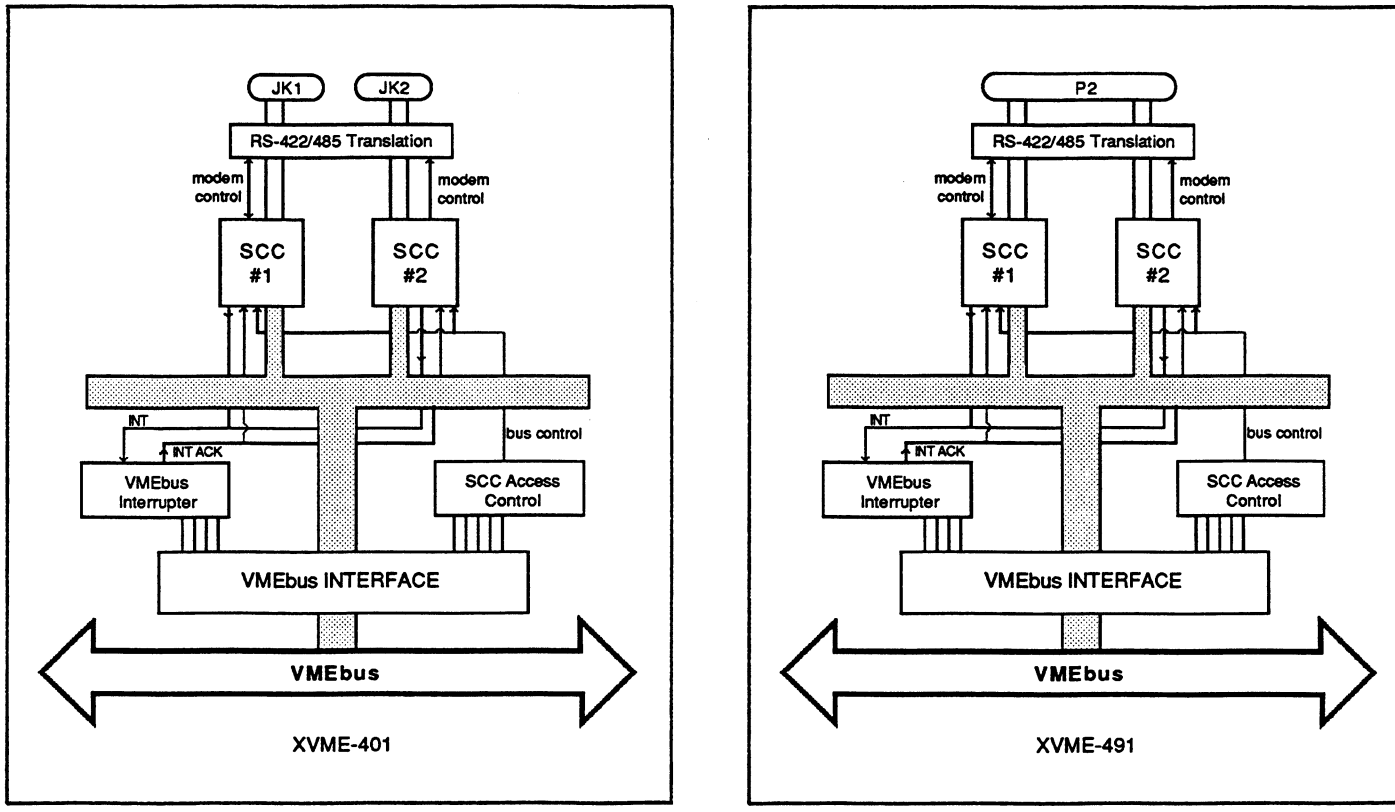


Figure 1-2. XVME-401 and XVME-491 Operational Block Diagrams

1.4 MODULE SPECIFICATIONS

The following is a list of the operational and environmental specifications for the XVME-400/401/490/491 Modules.

Table 1-1. XVME-400/401/490/491 Module Specifications

Characteristic	Specification
Number of Channels	4
Serial Device	Zilog 28530
Level Compatibility:	
XVME-400/490	RS-232C
XVME-401/491	RS-485/422A
Maximum Baud Rate:	
Internal, async	57.6 Kbytes
Internal, sync	500 Kbytes
External, async	57.6 Kbytes
External, sync	500 Kbytes
Modem Control Signals Available	
XVME-400/401/490	RTS, CTS, DCD, DTR
XVME-491	RTS, CTS, DCD
Power Requirements	
XVME-400/490	+5V @ 1.1 A typ., 1.3 A max. +12V @ 100 mA typ., 110 mA max.
XVME-401/491	+5V @ 1.4 A typ., 1.6 A max.
Temperature	
Operating	0 to 65°C (32 to 149°F)
Non-operating	-40 to 85°C (-40 to 158°F)
Humidity	5 to 95% RH non-condensing (Extremely low humidity may require protection against static discharge.)
Altitude	
Operating	Sea level to 10,000 ft. (3048 m)
Non-operating	Sea level to 50,000 ft. (15240 m)

Table 1-1. XVME-400/40 l/490/49 1 Module Specifications (cont.)

Characteristic	Specification
Vibration	
Operating	5 to 2000 Hz 0.0 15" peak-to-peak displacement 2.5 g peak acceleration
Non-operating	5 to 2000 Hz 0.030" peak-to-peak displacement 5.0 g peak acceleration
Shock	
Operating	30 g peak acceleration, 11 msec duration
Non-operating	50 g peak acceleration, 11 msec duration
VMEbus Compliance	- Complies with VMEbus Specification, IEEE 1014 - A16:D8(0) DTB Slave - Interrupt vector D08(0)DYN - I(1) to I(7) interrupter (STAT), ROAK - XVME-400/401: Single form factor XVME-490/491: Double form factor

VMEbus Timing:	Typ(ns)	Max(ns)
DSO Asserted to DTACK Asserted (Read)	650	800
DSO Asserted to DTACK Asserted (Write)	650	800
IACKIN Asserted to DTACK Asserted (IACK)	1100	1200
DSO Negated to DTACK Negated (All)	60	100
IACKIN Asserted to IACKOUT Asserted	300	400

Chapter 2

INSTALLATION

2.1 INTRODUCTION

This chapter explains how to configure an XVME-400/401/490/491 Module prior to installation in a VMEbus backplane. Included in this chapter is information on module base address selection jumpers, module interrupt level selection jumpers, +5V, tri-state jumpers, connector pinouts, and a brief outline of the physical installation procedure.

2.2 SYSTEM REQUIREMENTS

The XVME-400/40I Modules (single-high) or the XVME-490/491 Modules (double-high) are VMEbus-compatible modules. To operate, each must be properly installed in a VMEbus backplane.

The minimum system requirements for the operation of an XVME-400/401/490/491 Module are one of the following:

A) A host processor properly installed on the same backplane.

A properly installed system controller module which provides the following functions:

- Data Transfer Bus Arbiter
- System Clock Driver
- System Reset Driver
- Bus Timeout Module

O R

B) A host processor which incorporates the system controller functions on-board.

An example of such a controller subsystem is the XYCOM XVME-010 System Resource Module (SRM).

Prior to installing the XVME-400/401/490/491 Module, it will be necessary to configure several jumper options. These options are:

1) Module base address within the short I/O address space
2) Address modifier codes to which the module will respond
3) Interrupt level
4) +5, tri-state jumpers (XVME-401 only)

2.3 JUMPER/CONNECTOR LOCATIONS

The jumpers and connectors relevant to the installation of the XVME-400/401/490/491 Module are shown in Figures 2-1, 2-2, 2-3, and 2-4.

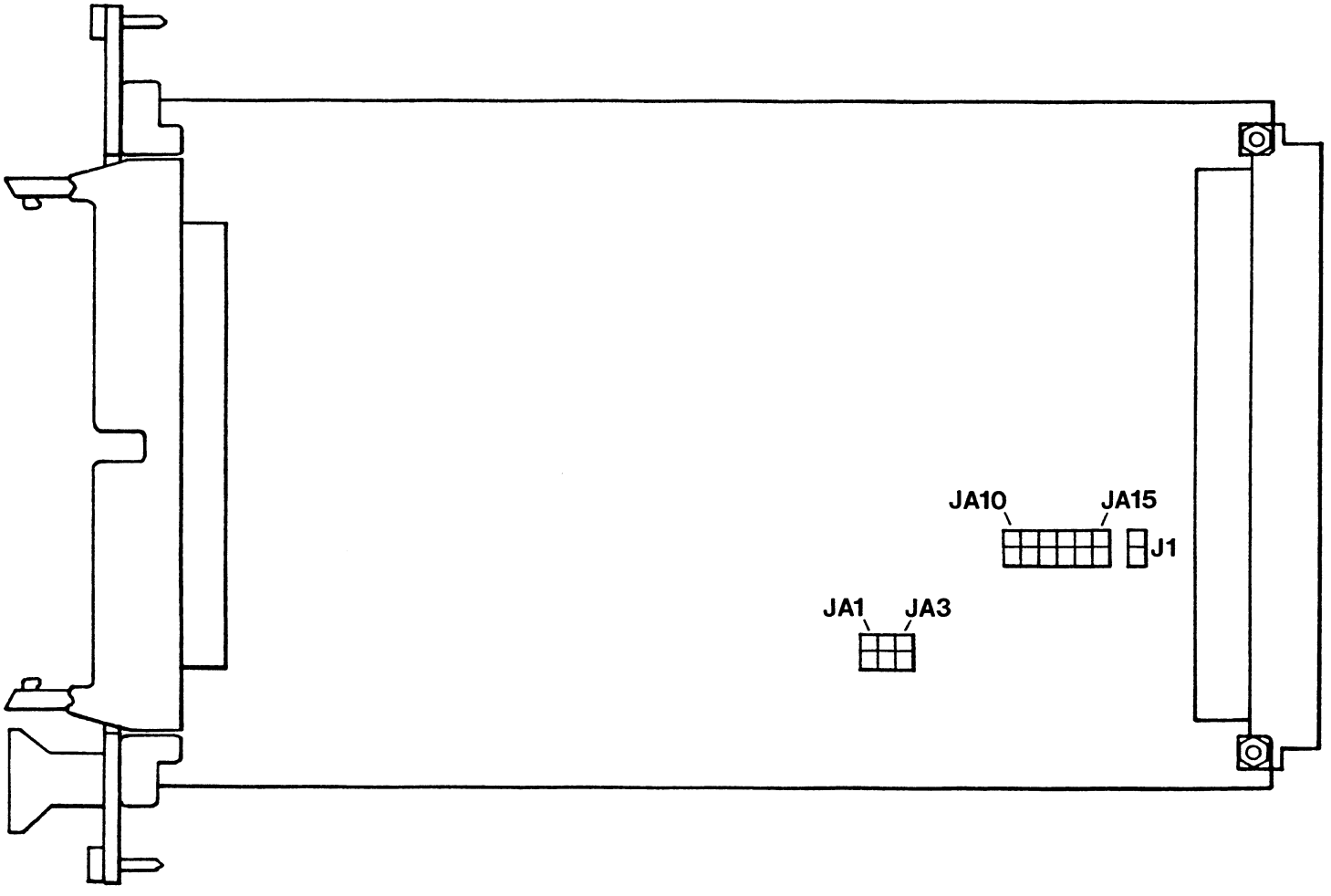


Figure 2-1. Jumper/Connector Locations on the XVME-400 Module

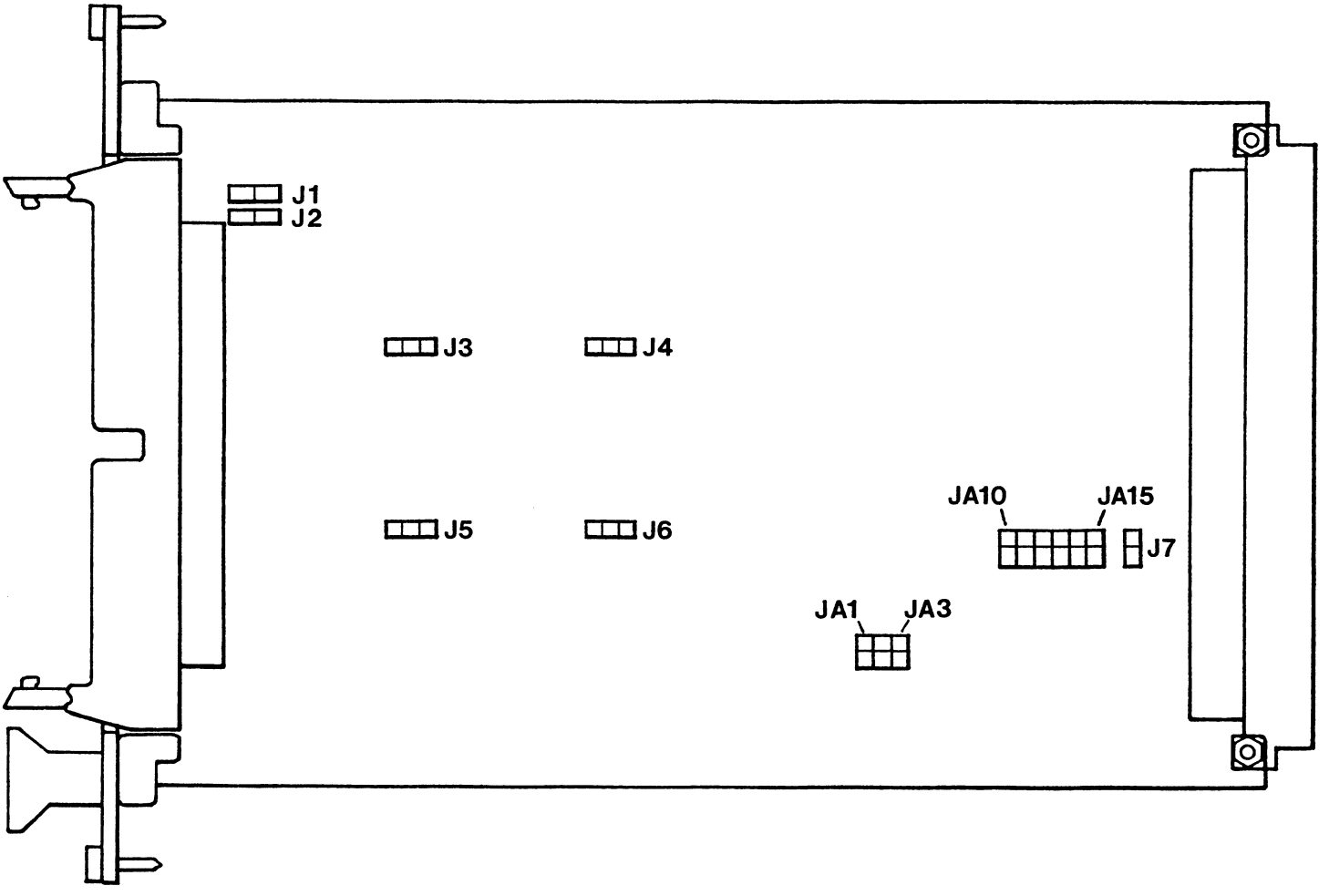


Figure 2-2. Jumper/Connector Locations on the XVME-401 Module

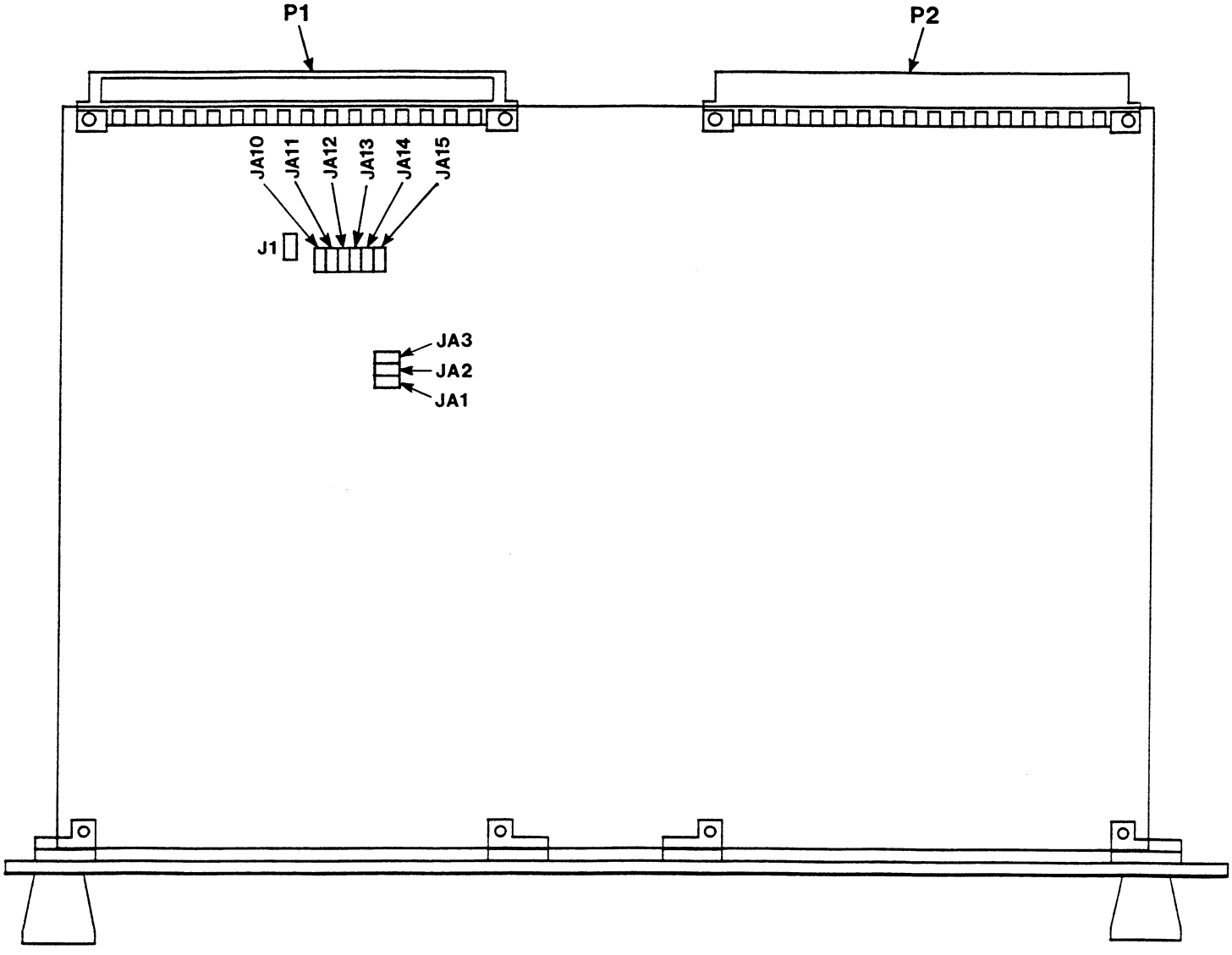


Figure 2-3. Jumper/Connector Locations on the XVME-490 Module

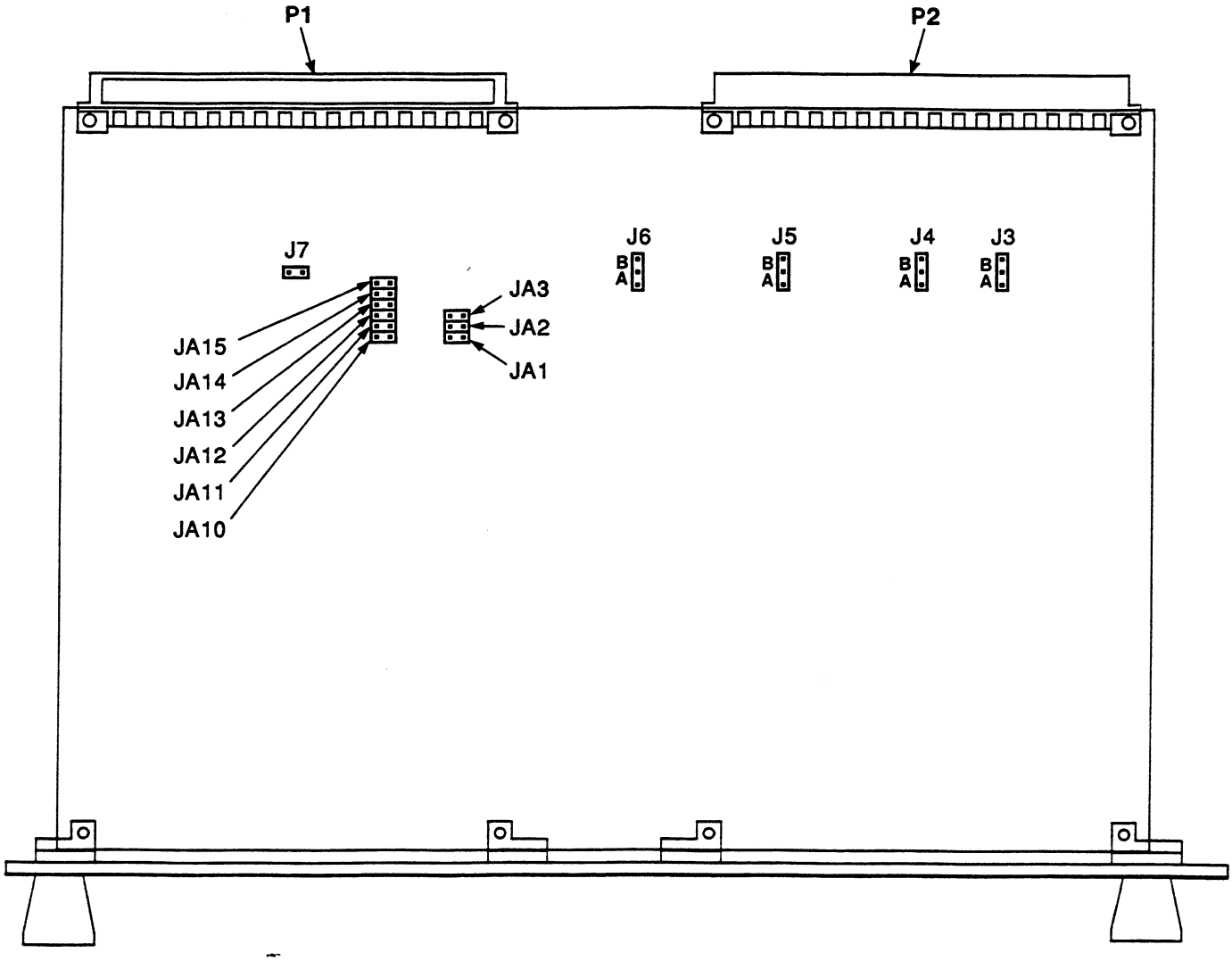


Figure 2-4. Jumper/Connector Locations on the XVME-491 Module

2.4 XVME-400/401/490/491 MODULE JUMPER LIST

Table 2-1. XVME-400 and XVME-490 Jumper List

Jumper	Use
J1	Determines whether the module will respond to supervisory or supervisory and non-privileged short I/O VMEbus cycles (refer to Section 2.4.2 of this manual).
JAl0-JAI5	Selects module base address on any one of the 64 1 Kbyte boundaries within the short I/O address space (refer to Section 2.4.1 of this manual).
JAI-JA3	Selects the VMEbus interrupt level for the module (refer to Section 2.4.3 of this manual).

Table 2-2. XVME-401 and 491 Jumper List

Jumper	Use
Jl and J2	Brings the +5V supply to front-edge connectors JKl and JK2, respectively (XVME-401 only; refer to Section 2.4.4).
J3-J6	Allows tri-stating of any of the channels (refer to Section 2.4.5).
J7	Determines whether the module will respond to supervisory or supervisory and non-privileged short I/O VMEbus cycles (refer to Section 2.4.2).
JAl0-JAI5	Selects module base address on any one of the 64 1 Kbyte boundaries within the short I/O address space (refer to Section 2.4.1).
JAI-JA3	Selects the VMEbus interrupt level for the module (refer to Section 2.4.3).

2.4.1 Base Address Jumpers (JA10-JA15)

The XVME-400/401/490/491 Module can be configured to be addressed at any one of the 64 1 Kbyte boundaries within the VME Short I/O address space by using jumpers JAl0 through 5 (see Figures 2-1, 2-2, 2-3, and 2-4 for the location of the jumpers on the board) as shown above. Table 2-3 shows the Base Address Jumper Options.

Table 2-3. Base Address Jumper Options

JA15	JA14	JA13	JA12	JA11	JA10	Base Address of Module
In	In	In	In	In	In	0000H
In	In	In	In	In	Out	0400H
In	In	In	In	Out	In	0800H
In	In	In	In	Out	Out	0C00H
In	In	In	Out	In	In	1000H
In	In	In	Out	In	Out	1400H
In	In	In	Out	Out	In	1800H
In	In	In	Out	Out	Out	1C00H
In	In	Out	In	In	In	2000H
In	In	Out	In	In	Out	2400H
In	In	Out	In	Out	In	2800H
In	In	Out	In	Out	Out	2C00H
In	In	Out	Out	In	In	3000H
In	In	Out	Out	In	Out	3400H
In	In	Out	Out	Out	In	3800H
In	In	Out	Out	Out	Out	3C00H
In	Out	In	In	In	In	4000H
In	Out	In	In	In	Out	4400H
In	Out	In	In	Out	In	4800H
In	Out	In	In	Out	Out	4C00H
In	Out	In	Out	In	In	5000H
In	Out	In	Out	In	Out	5400H
In	Out	In	Out	Out	In	5800H
In	Out	In	Out	Out	Out	5C00H
In	Out	Out	In	In	In	6000H
In	Out	Out	In	In	Out	6400H
In	Out	Out	In	Out	In	6800H
In	Out	Out	In	Out	Out	6C00H
In	Out	Out	Out	In	In	7000H
In	Out	Out	Out	In	Out	7400H
In	Out	Out	Out	Out	In	7800H
In	Out	Out	Out	Out	Out	7C00H
Out	In	In	In	In	In	8000H
Out	In	In	In	In	Out	8400H
Out	In	In	In	Out	In	8800H
Out	In	In	In	Out	Out	8C00H
Out	In	In	Out	In	In	9000H
Out	In	In	Out	In	Out	9400H
Out	In	In	Out	Out	In	9800H
Out	In	In	Out	Out	Out	9C00H
Out	In	Out	In	In	In	A000H
Out	In	Out	In	In	Out	A400H
Out	In	Out	In	Out	In	A800H
Out	In	Out	In	Out	Out	AC00H
Out	In	Out	Out	In	In	B000H
Out	In	Out	Out	In	Out	B400H
Out	In	Out	Out	Out	In	B800H
Out	In	Out	Out	Out	Out	BC00H
Out	Out	In	In	In	In	C000H
Out	Out	In	In	In	Out	C400H
Out	Out	In	In	Out	In	C800H
Out	Out	In	In	Out	Out	CC00H
Out	Out	In	Out	In	In	D000H
Out	Out	In	Out	In	Out	D400H
Out	Out	In	Out	Out	In	D800H
Out	Out	In	Out	Out	Out	DC00H
Out	Out	Out	In	In	In	E000H
Out	Out	Out	In	In	Out	E400H
Out	Out	Out	In	Out	In	E800H
Out	Out	Out	In	Out	Out	EC00H
Out	Out	Out	Out	In	In	F000H
Out	Out	Out	Out	In	Out	F400H
Out	Out	Out	Out	Out	In	F800H
Out	Out	Out	Out	Out	Out	FC00H

2.4.2 Address Modifier Jumper (Jl or J7)

Each XVME-400/401/490/491 Module has one jumper that determines which address modifier codes it will respond to. This jumper is Jl on the XVME-400/490 and J7 on the XVME-401/491 (see Figures 2-1, 2-2, 2-3, and 2-4 for the jumper location). When this jumper is in, the module will respond to supervisory short I/O bus cycles only. When this jumper is out, the module will respond to both non-privileged and supervisory short I/O bus cycles. Table 2-4 shows the relationship between this jumper and the address modifiers.

Table 2-4. Addressing Options

Jumper J1 (XVME-400/490), or J7 (XVME-401/491)	**Address Modifier to which the XVME-400/40l/490/491 Module will respond**
In	(2DH) Supervisory only
Out	(2DH) Supervisory or (29H) Non-privileged

2.4.3 Interrupt Level Selection Jumpers (JAl-JA3)

The XVME-400/401/490/491 Module can either be configured to generate VMEbus interrupts at levels 1-7 or the module interrupt capability can be completely disabled. Table 2-5 shows how jumpers JAl-JA3 are used to determine the interrupt level status for the XVME-400/40l/490/491 Module.

Table 2-5. Interrupt Level Jumper Positions

JA3	**JA2**	**JA1**	**Interrupt Level Selected**
In	In	In	None, VMEbus Interrupter disabled
In	In	out	Level 1
In	out	In	Level 2
In	out	out	Level 3
out	In	In	Level 4
out	In	out	Level 5
out	out	In	Level 6
out	out	out	Level 7

The module is shipped from the factory with jumpers JAl, JA2, and JA3 installed.

NOTE

If the module is never required to generate interrupts, JAI, JA2, and JA3 should be installed to ensure that a programming bug will not generate a VMEbus interrupt.

2.4.4 +5V Power Supply (Jl, J2; XVME-401 only)

On the XVME-401, jumpers Jl and J2 control whether the +5V supply is brought out to front-edge connectors JKl and JK2. Table 2-6 indicates the functions of these jumpers.

Table 2-6. +5V Jumpers (XVME-401 only)

Jumper	Use
J1	If Jl is installed, +5V will be connected to JKl (pin 47). If Jl is removed, JKI-47 will float.
J2	If J2 is installed, +5V will be connected to JK2 (pin 47). If J2 is removed, JK2-47 will float.

The +5V signals on the front-edge connector could be used to provide external line termination by being used as a pull-up voltage, or for biasing.

2.4.5 Tri-stating the Serial Channels (J3-J6; XVMIE-401/491 only)

To facilitate multidrop configurations, all drivers associated with a particular communication channel may be tri-stated or enabled via SCC output pin RTS*. Each channel has its own jumper to determine how the RTS* output affects line driver enabling.

When a channel's jumper is in the A position, the line drivers associated with that channel for TT, RS, SD, and TR will be controlled by RTS*. When RTS* is negated (high voltage), all line drivers associated with that channel will be tri-state. When RTS* is asserted, all line drivers associated with that channel will be enabled. When a channel's jumper is in the B position, the line drivers associated with that channel will be enabled, regardless of the state of the SCC output RTS*.

The jumper numbers related to the serial channel numbers are shown below and are all shipped in the B position:

J3 Channel 3
J4 Channel 2
J5 Channel 1
J6 Channel 0

2.4.6 Daisy Chain Signals

Each slot in the VME backplane must propagate the Daisy Chain signals to the next backplane slot. This occurs automatically if boards are installed in the slots. Where boards are not installed, the appropriate backplane jumpers must be installed to continue the signal path.

NOTE

Boards and jumpers should never both be installed in any one slot.

2.5 MODULE CONNECTORS

The location of the module connectors is shown in Table 2-7 (connector pinouts for P1 are shown in Appendix A).

Table 2-7. Module Connector Locations

Module	Connectors	
	Front Edge	Rear Edge
XVME-400 & 401	JK1 & JK2	P1
XVME-490 & 491		P1, P2

2.5.1 JK1 and JK2 Connectors

The XVME-400 and XVME-401 have two 50-pin connectors, designated as JK1 and JK2, which are accessible through the front panel (see Figure 2-5).

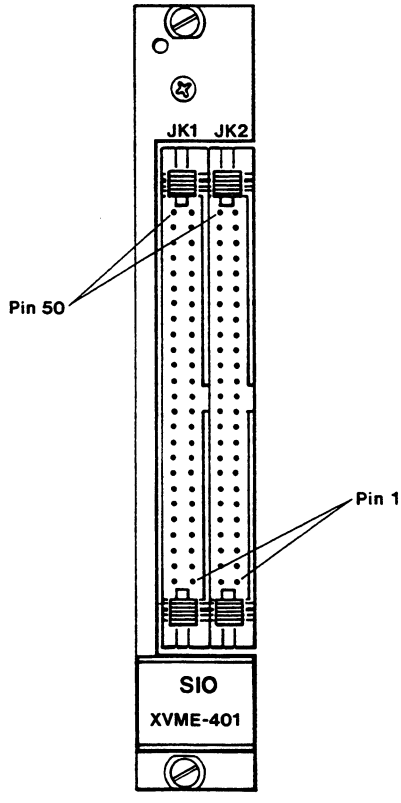


Figure 2-5. XVME-400/401 Front-edge Connector

On the XVME-400/401, connector JKl carries the signals for Channels 0 and 2, while connector JK2 carries the signals for Channels 1 and 3. On the XVME-490/491, the signals for all four channels are carried on connector P2. All channels on all modules are configured as DTE.

Sources of JKl /JK2. or P2 Connector Output Signals (one set for each serial channel)

TXD/SD SCC output pin TXD drives a line driver. Driver output is sent to this pin.

RTS/RS SCC output pin RTS* drives a line driver. Driver output is sent to this pin.

TXC/TT SCC output pin TRXC drives a line driver. Driver output is sent to this pin.

DTR/TR SCC output pin DTR* drives a line driver. Driver output is sent to this pin.

NOTE

The RS232C signal names (XVME-400/490) are given to the left of the slash, and the RS-485/422A signal names to the right (XVME-40l/491).

All line drivers invert the signal. For modem control lines, writing a 1 to the appropriate SCC writer register bit will cause the output to be asserted. For TXD/SD and TXC/TT, the polarity defined by RS-232C or RS-485 is provided.

Destinations of JKl /JK2. or P2 Connector Input Signals (one set for each serial channel)

RXD/RD This input pin is buffered by a line receiver and is driven to the SCC input pin RXD.

CTS/CS This input pin is buffered by a line receiver and is driven to the SCC input pin CTS*.

RXC/RT This input pin is buffered by a line receiver and is driven to the SCC input pin RTXC.

DCD/RR This input pin is buffered by a line receiver and is driven to the SCC input pin DCD*.

All line receivers invert the signal. For modem control lines, a 1 will be read from the appropriate SCC read control register bit when the input is asserted. For RXD/RD and RXC/RT, the polarity defined by RS-232C or RS-485 is provided.

2.5.1.1 JKl and JK2 Connector Pinouts on the XVME-400 (RS-232C)

Table 2-8 shows the XVME-400 pinout connectors JKl and JK2. These signals meet the RS-232C specifications.

Table 2-8. XVME-400 Front Edge Connector Pin Definitions

Pin Number	JKl Signal	JK2 Signal	Signal	Direction
3	TXDO	TXDl	Transmit Data	OUT
5	RXDO	RXDl	Receive Data	IN
7	RTSO	RTSl	Request To Send	OUT
8	RXCO Ch. 0	RXCl Ch. 1	Receiving Clock	IN
9	CTSO	CTSl	Clear To Send	IN
13	GND	GND	Ground	
14	DRTO	DTRl	Data Terminal Ready	OUT
15	DCDO	DCDl	Data Carrier Detected	IN
22	TXCO	TXCI	Transmitting Clock	OUT
28	TXD2	TXD3	Transmit Data	OUT
30	RXD2	RXD3	Receive Data	IN
32	RTS2	RTS3	Request To Send	OUT
33	RXC2 Ch. 2	RXC3 Ch. 3	Receiving Clock	IN
34	CTS2	CTS3	Clear To Send	IN
38	GND	GND	Ground	
39	DTR2	DTR3	Data Terminal Ready	OUT
40	DCD2	DCD3	Data Carrier Detected	IN
47	TXC2	TXC3	Transmitting Clock	OUT

NOTE

All XVME-400 signal names are in the form XXXN where "N" is the serial channel number and '(XXX" is the name of the signal.

All JKl and JK2 pin numbers not referenced are not connected.

The pinouts of JKl and JK2 allow a 50-conductor flat cable to be connected, split into two 25-conductor sections, and have 25-pin D-type connectors installed on the two 25-conductor sections. The position of the signals relevant to the 25-pin D-type connectors will be in accordance with the RS-232C definition (no line transitions are required):

TXD	Pin 2	DCD Pin 8
RXD	Pin 3	RXC Pin 17
RTS	Pin 4	DTR Pin 20
CTS	Pin 5	TXC Pin 24
GND	Pin 7	

2.5.1.2 JKl and JK2 Connector Pinouts on the XVME-401 (RS-485/422A)

Table 2-9 shows the XVME-401 pinouts for connectors JKl and JK2. These signals meet the RS-485/422A specifications.

Table 2-9. XVME-401 Front Edge Connector Pin Definitions

Pin Number	JKl Signal	JK2 Signal	Signal	Direction
1	SDOB	SDlB	Transmit Data	OUT
2	SDOA	SDlA	Transmit Data	OUT
5	RDOB	RDlB	Receive Data	IN
6	RDOA	RDIA	Receive Data	IN
7	RSOB	RSlB	Request To Send	OUT
8	RSOA	RSlA	Request To Send	OUT
9	RTOB	RTlB	Receive Clock	IN
10	RTOA Ch. 0	RTlA Ch. 1	Receive Clock	IN
11	CSOB	CSlB	Clear To Send	IN
12	CSOA	CSlA	Clear To Send	IN
16	TROB	TRIB	Data Terminal Ready	OUT
17	TROA	TRlA	Data Terminal Ready	OUT
18	RROB	RRlB	Data Carrier Detect	IN
19	RROA	RRlA	Data Carrier Detect	IN
20	TTOB	TTlB	Transmit Clock	OUT
21	TTOA	TTlA	Transmit Clock	OUT
24	SC0	SC1	Logic Ground	GND
25	SGO	SGl	Logic Ground	GND
26	SD2B	SD3B	Transmit Data	OUT
27	SD2A	SD3A	Transmit Data	OUT
30	RD2B	RD3B	Receive Data	IN
31	RD2A	RD3A	Receive Data	IN
32	RS2B	RS3B	Request To Send	OUT
33	RS2A	RS3A	Request To Send	OUT
34	RT2B	RT3B	Receive Clock	IN
35	RT2A	RT3A	Receive Clock	IN
36	CS2B Ch. 2	CS3B Ch. 3	Clear To Send	IN
37	CS2A	CS3A	Clear To Send	IN
41	TR2B	TR3B	Data Terminal Ready	OUT
42	TR2A	TR3A	Data Terminal Ready	OUT
43	RR2B	RR3B	Data Carrier Detect	IN
44	RR2A	RR3A	Data Carrier Detect	IN
45	TT2B	TT3B	Transmit Clock	OUT
46	TT2A	TT3A	Transmit Clock	OUT
47 (2)	+5v	+5v		OUT
49	SC2	SC3	Logic Ground	GND
50	SG2	SG3	Logic Ground	GND

NOTE

All XVME-401 signal names are in the form "XXNZ", where "N" is the channel number, **"Z"** is A or B based on the polarity of the differential signal (as defined by RS-485), and "XX" is the name of the signal. Also see Section 2.4.4.

All JKl and JK2 pin numbers not referenced are not connected.

2.5.2 Pl and P2 Connectors

The Pl and P2 connectors are the same physical type and have the same number of pins. Both are 96-pin connectors consisting of three rows of 32 pins each. Like Pl, P2 is mounted at the rear edge of the module. The pins for Pl contain the standard address, data, and control signals necessary for the operation of VMEbus-defined NEXP modules. (The signal definitions and pin-outs for connector Pl are found in Appendix A of this manual.) The PI connector is designed to mechanically interface with a VMEbus defined P 1 backplane.

The P2 connector (XVME-490/491 only) is a standard VMEbus P2 backplane connector. It is designed to interface with a VMEbus defined P2 backplane.

2.5.2.1 P2 Connector Pinouts on the XVME-490 (RS-232C)

Table 2-10 shows the XVME-490 pinouts for connector P2. These signals meet the RS-232C and VMEbus specifications.

Table 2-10. XVME-490 Rear Edge P2 Connector Pin Definitions

Pin #	Row A Signal	Row B Signal	Row C Signal
1	TXDO	vcc	GND
2	RXDO	GND	GND
3	RTSO	NC	GND
4	RXCO Ch. 0	NC	GND
5	CTSO	NC	GND
6	DTRO	NC	GND
7	DCDO	NC	GND
8	TXCO	NC	GND
9	TXDl	NC	GND
10	RXDl	NC	GND
11	RTSl	NC	GND
12	RXCI Ch.1	GND	GND
13	CTSl	vcc	GND
14	DTRI	NC	GND
15	DCDl	NC	GND
16	TXCI	NC	GND

Table 2-10. XVME-490 Rear Edge P2 Connector Pin Definitions (Cont'd)

Pin #	Row A Signal	Row B Signal	Row C Signal
17	TXD2	NC	GND
18	RXD2	NC	GND
19	RTS2	NC	GND
20	RXC2 Ch. 2	NC	GND
21	CTS2	NC	GND
22	DTR2	GND	GND
23	DCD2	NC	GND
24	TXC2	NC	GND
25	TXD3	NC	GND
26	RXD3	NC	GND
27	RTS3	NC	GND
28	RXC3 Ch. 3	NC	GND
29	CTS3	NC	GND
30	DTR3	NC	GND
31	DCD3	GND	GND
32	TXC3	vcc	GND

NOTE

All P2 signal names are of the form "XXXN" where "N" is the serial channel number and "XXX' is the name of the signal. Signals with the same "XXX" function identically with respect to the particular channel.

2.5.2.2 P2 Connector Pinouts on the XVME-491 (RS-485/422A)

Table 2-11 shows the XVME-491 pinouts for connector P2. These signals meet the RS-485/422A and VMEbus specifications.

T-able 2-11. XVME-491 Rear Edge P2 Connector Pin Definitions

Pin #	Row A Signal	Row B Signal	Row C Signal
1	TXDO+	vcc	TXDO-
2	TXCO+	GND	TXCO-
3	RTSO+	NC	RTSO-
4	RXDO+ Ch. 0	NC	RXDO-
5	RXCO+	NC	RXCO-
6	CTSO+	NC	CTSO-
7	DCDO+	NC	DCDO-
8	GND	NC	GND
9	TXD1+	NC	TXDI-
10	TXC1+	NC	TXCl-
11	RTSl+	NC	RTSl-
12	RXDl+ Ch. 1	GND	RXDl-
13	RXCl+	vcc	RXCl-
14	CTSl+	NC	CTSl-
15	DCDl+	NC	DCDI-
16	GND	NC	GND
17	TXD2+	NC	TXD2-
18	TXC2+	NC	TXC2-
19	RTS2+	NC	RTS2-
20	RXD2+ Ch. 2	NC	RXD2-
21	RXC2+	NC	RXC2-
22	CTS2+	GND	CTS2-
23	DCD2+	NC	DCD2-
24	GND	NC	GND
25	TXD3+	NC	TXD3-
26	TXC3+	NC	TXC3-
27	RTS3+	NC	RTS3-
28	RXD3+ Ch. 3	NC	RXD3-
29	RXC3+	NC	RXC3-
30	CTS3+	NC	CTS3-
31	DCD3+	GND	DCD3-
32	GND	vcc	GND

NOTE

All XVME-401 signal names are in the form "XXNZ", where "N" is the channel number, "Z" is + or - based on which half of the signal it is, and "XX" is the name of the signal.

2.6 MODULE INSTALLATION

XYCOM XVME modules are designed to comply with all physical and electrical VMEbus backplane specifications. The XVME-400/401 Modules are single-high and single-wide and, as such, only require the Pl backplane. The XVME-490/491 Modules are double-high and single-wide, and use the PI and P2 backplane.

CAUTION

Never attempt to install or remove any boards before turning off the power to the bus, and all related external power supplies.

Prior to installing a module, determine and verify all relevant jumper configurations, and all connections to external devices or power supplies. (Check the jumper configuration against the diagrams and lists in this manual.)

To install a board in the cardcage, perform the following steps:

1) Make certain that the particular cardcage slot which you are going to use is clear and accessible.

2) Center the board on the plastic guides in the slot so that the handle on the front panel is towards the bottom of the cardcage (XVME-400/401 only).

3) Push the card slowly toward the rear of the chassis until the connectors engage (the card should slide freely in the plastic guides).

4) Apply straight-forward pressure to the handle located on the front panel of the module until the connector is fully engaged and properly seated.

NOTE

Do not use excessive pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

5) Once the board is properly seated, secure it to the chassis by tightening the two machine screws at the top and bottom of the board.

Chapter 3

MODULE PROGRAMMING

3.1 INTRODUCTION

This chapter will discuss the addressing and initialization procedures for programming the XVME-400/40l/490/491 Modules. In order to demonstrate the correct sequence of initialization for the serial channels contained in the SCC chips, two programming examples (with comments) have been incorporated in this chapter. For a complete explanation of how to program and maximize the functionality of the SCC chip, refer to the accompanying SCC Manual.

Each module contains four serial communication channels, designated as channels 0, 1,2, and 3. Each SCC has two serial channels designated by Zilog as channels A and B. The SCC channels map into the module channels as follows:

Module Channel Number	SCC Channel	Priority
0	SCC #1, Channel A	Highest
1	SCC #1, Channel B	
2	SCC #2, Channel A	
3	SCC #2, Channel B	Lowest

Throughout this document, the module channel number (0, 1, 2, 3) will be referenced.

For interrupt operation, the serial channels are prioritized, with channel 0 having the highest priority and channel 3 having the lowest priority. Therefore, for a given application, the serial links running at higher data rates should be assigned to module channels with higher interrupt priority.

3.2 MODULE ADDRESSING

The XVME-400/401/490/491 Modules are designed to be addressed within the VMEbus-defined 64 Kbyte short I/O address space. When the XVME-400/401/490/491 Module is installed in the system it will occupy a 1 Kbyte block of the short I/O address space. The base address decoding scheme for the XVME I/O modules is such that the starting address for each board resides on a 1 Kbyte boundary. Thus, there are 64 possible locations (1 Kbyte boundaries) in the short I/O address space which could be used as the base address for the XVME-400/401/490/491 Module. (Refer to Section 2.4.1 for the list of base addresses and their corresponding jumper configurations).

All register locations within the SCC devices are given specific addresses which are offset from the module base address. Thus, a specific register address in one of the SCC chips can be accessed by adding the specific register offset to the module base address. For example, the offset specified for the Serial Channel 2 Data Register is 07H, and if the module base address is jumpered to 1000H, the register can be accessed at 1007H.

Module Base Address		Register Offset		Serial Channel 2 Data Register
1000H	+	07H	=	1007H

NOTE

The XVME-400/401/490/491 is an odd byte only slave, and as such, the module will not respond to even address, single-byte accesses. However, word accesses may be used, with the understanding that only the odd byte of the word is used to exchange data. If word accesses are used, the register offsets listed in Table 3-1 would all be decremented by 1.

Table 3-1 lists the offsets for the internal registers of all four serial channels on the XVME-400 (two channels per SCC serial chip).

Table 3-1. Register Offsets

Off set Address		Module Register	
Hex	**Decimal**		
1	1	Serial Channel 3 Control Register	(SCC #2 Channel B)
3	3	Serial Channel 3 Data Register	(SCC #2 Channel B)
5	5	Serial Channel 2 Control Register	(SCC #2 Channel A)
7	7	Serial Channel 2 Data Register	(SCC #2 Channel A)
9	9	Serial Channel 1 Control Register	(SCC #l Channel B)
B	11	Serial Channel 1 Data Register	(SCC #l Channel B)
D	13	Serial Channel 0 Control Register	(SCC #l Channel A)
F	15	Serial Channel 0 Data Register	(SCC #l Channel A)

The registers in the 8530 are accessed in a two-step process. The first step is to write a pointer to one of the four control registers listed in Table 3-l. After the pointer is written to a control register, the next read or write to the same control register will access the desired 8530 register. Refer to the 8530 Manual for a description of the 8530 registers and their pointers.

Single-step access of a data register is performed by reading or writing to any of the four data registers. The XVME-400/401/490/491 will automatically set D/C high and will access the 8530 registers RRS or WRS directly, independent of the state of the pointer bits.

3.3 MODULE INTERRUPT SOURCES

There are twelve sources of interrupts on the XVME-400/401/490/491 (three sources from each serial channel). When enabled, each of these sources can generate VMEbus interrupts on the level specified by jumpers JAI-JA3. The interrupt sources are prioritized during the VMEbus IACK cycle, as shown in Table 3-2.

Table 3-2. Priority of Local Interrupt Sources

Channel	Interrupt Source	Priority
0	Receive Character Available	Highest
0	Transmit Buffer Empty	
0	External/Status Change	
1	Receive Character Available	
1	Transmit Buffer Empty	
1	External/Status Change	
2	Receive Character Available	
2	Transmit Buffer Empty	
2	External/Status Change	
3	Receive Character Available	
3	Transmit Buffer Empty	
3	External/Status Change	Lowest

When the module responds to a VMEbus IACK cycle, the IACK vector is acquired from the appropriate SCC chip and driven onto the VMEbus. Since each SCC can produce 8 vectors, SCC IACK vector register (WR2) must be initialized before interrupts are enabled. When programmed to include status in the IACK vector (WR9:DO=l), the status high/low bit (WR9:D4) determines whether IACK vector bits 3,2,1 or bits 4,5,6 will contain status information. The status information returned in IACK vector is shown in Table 3-3 on the following page:

Table 3-3. IACK Vector Containing the Status

IACK Vector (WR9:D4=0)								IACK Vector (WR9:D4=1)								Interrupt Source
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	VMEbus Data Bit
X	X	X	X	0	0	0	X	X	0	0	0	X	X	X	X	Ch.1 or 3 Transmit Buffer Empty
X	X	X	X	0	0	1	X	X	1	0	0	X	X	X	X	Ch.1 or 3 External Status/Change
X	X	X	X	0	1	0	X	X	0	1	0	X	X	X	X	Ch.1 or 3 Receive Character Available
X	X	X	X	0	1	1	X	X	1	1	0	X	X	X	X	Ch.1 or 3 Special Receive Condition
X	X	X	X	1	0	0	X	X	0	0	1	X	X	X	X	Ch.0 or 2 Transmit Buffer Empty
X	X	X	X	1	0	1	X	X	1	0	1	X	X	X	X	Ch.0 or 2 External Status/Change
X	X	X	X	1	1	0	X	X	0	1	1	X	X	X	X	Ch.0 or 2 Receive Character Available
X	X	X	X	1	1	1	X	X	1	1	1	X	X	X	X	Ch.0 or 2 Special Receive Condition

X = Status bit returned (from the SCC's IACK Vector Register WR2).

Table 3-3 shows the vectors for a single SCC. The vector written to SCC #1's WR2 register (Channel 0 or 1) will be used for serial channels 0 and 1. The vector written to SCC #2's WR2 register (Channel 2 or 3) will be used for serial channels 2 and 3.

The interrupt daisy chain feature of the SCC is used to arbitrate IACK cycles between the two SCCs. SCC #1 has its IEO pin connected to SCC #2's IEI pin. It is suggested that the DLC bit (WR9:D2) be set to zero to enable the IEO output pin. The MIE bit (WR9:D3) can then be used as a master interrupt enable for the individual SCCs. This mode of operation keeps the operation of both SCCs symmetric.

At the end of the ISR routine, the Reset Highest IUS command must be issued to enable lower priority interrupts.

3.3.1 Receive Character Available Interrupts

Each of the four channels has its own receive character available: IE, IP, and IUS internal bits. The IE bit is set by writing to WR1:D4, D3, and D2. If interrupts are enabled, the IP bit will be set whenever a received character is in the receive FIFO. (The state of this bit can be read from RR3:D2,D5.) The IP bit is reset by reading the channel's data register.

Special Receive Conditions
There are two different IACK vectors for the receive character available interrupts: the Receive Character Available IACK vector and the Special Receive Condition IACK vector. When there are no special conditions associated with the received character on top of the

FIFO, the Receive Character Available IACK vector will be acquired. If there is a special receive condition associated with the character on top of the FIFO, the Special Receive Condition IACK vector will be acquired.

There are four special receive conditions:

1) Receive overrun
2) Framing error (ASYNC only)
3) End of frame (SLDLC only)
4) Parity error (if WRl:D2=1)

For interrupt driven operation, it is suggested that an interrupt on all receive characters or special conditions be programmed along with programming parity errors as a special condition. When programmed in this mode, and the receive character available IACK vector is acquired, it is guaranteed that no special conditions exist for the received byte on top of the FIFO. Therefore, RR1 does not have to be checked after every receive byte. This eliminates two VMEbus cycles from the receive character interrupt service routine.

When a special receive condition IACK vector is acquired, the following sequence should be executed in the specified order:

1) Read RR1 to determine the source of special condition.
2) Issue reset error command in WRO to clear errors.
3) Read the data register.

3.3.2 Transmit Buffer Empty Interrupts

Each of the four channels has its own Transmit Character available: IE, IP, and IUS internal bits. The IE bit is set (i.e., transmit buffer interrupts are enabled) by setting WRl:Dl. If these interrupts are enabled, two events can cause this IP to become set: when the transmit buffer is ready to receive a byte (RRO:D2=1), and after the CRC is sent in synchronous modes (RRO:D2=0). The IP is reset by writing to the data register or by issuing the Reset TxINT Pending command WRO.

3.3.3 External/Status Interrupts

There are six sources of interrupts that share this IP:

1) Break/Abort
2) Underrun/EOM
3) CTS
4) DCD
5) Sync/Hunt
6) Zero Count

Each of these sources has a separate enable bit in WR15 and has a separate status bit in RRO. The master external/status interrupt enable bit is WRl:DO. In general, when a status bit changes state and is enabled, the external/status IP will be set and cause an interrupt. The IP is reset by issuing the Reset External/Status Interrupt command in WRO.

3.4 CLOCKING OPTIONS

This section describes the transmit and receive clocking options for the serial channels. It applies to all four independently configurable serial channels.

3.4.1 Hardware Configurations

The SCC receive clock input pin, RTXC, is driven from line receivers which are connected to the JK RT input (see Section 2.5). Therefore, the frequency of SCC pin RTXC is determined by the external clock connected to the RXC/RT input pin. This clock input signal will be referred to as RXC/RT in this section. The crystal oscillator feature of the SCC is not used.

The SCC transmit clock pin, TRXC, is used as an output. It is buffered by line drivers and driven to a TXC/TT output on a front edge connector. The SCC pin TRXC must be programmed as an output (WRl 1) and must not be selected as an internal SCC clock source. This clock output signal is referred to as TXC/TT in this section.

In all possible clocking combinations, the polarities of the clock signals TXC/TT and RXC/RT are in accordance with the RS-232C or RS-485 standards.

The SCC's clock pin PCLK is connected to a 3.6864 MHz clock. This frequency allows the baud rate generator to produce most of the popular baud rates used for serial communications.

3.4.2 Baud Rate Generator

The SCC contains a programmable baud rate generator whose output can be used as internal timing sources. The baud rate generator's clock input may be programmed to connect to either the RXC/RT signal or PCLK (WR14). A 16-bit time constant can be programmed into WR13 (most significant byte) and WR12 (least significant byte) to select the baud rate generator's output frequency. The following equations show the baud rate generator's output frequency as a function of the time constant, and vice versa:

If baud rate generator input is RXC or RT (WR14:Dl=O):

Time Constant = (Frequency of RXC/(2 * CM * Baud Rate)) -2
Baud Rate = Frequency of RXC/(2 * CM * (Time Constant + 2))

If baud rate generator input is PCLK (WR14:Dl=l): (PCLK = 3.6864 MHz)

Time Constant = (1.8432 MHz/(CM * Baud Rate)) -2
Baud Rate = 1.8432 MHz/(CM * (Time Constant + 2))

In the above equations, CM is the clock multiplier used by the transmitter and receiver (i.e., CM=1 6 for X 16 clock multiplier).

The output of the baud rate generator can be used as the transmitter clock source and/or the receiver clock source, and it may also be sent to the TXC/TT output. Any combination of these three may be used.

3.4.2.1 Programming the Baud Rate Generator

The following steps should be followed in the specified order to program the baud rate generator:

1) Disable the baud rate generator (WR14:D0-0).
2) Load WR12 and WR13 with the desired time constant.
3) Select baud rate generator clock source:
   WR14:Dl = 0 for RXC/RT
   WR14:Dl = 1 for PCLK
4) Enable the baud rate generator, WR14:D0=l.

3.4.2.2 Time Constant Examples

The following tables show the time constants required for popular baud rates when PLCK is used as the baud rate generator input. Two tables are shown, one for synchronous (1X clock) and one for asynchronous (16X clock). These particular constants are shown for illustration only. Any time constant may be used.

Table 3-4. Typical Time Constraints for Synchronous (xl) Clock

Baud Rate	Time Constant (Base 10)	WR13 Value (Hex)	WR12 Value (Hex)
76.8 K	22	00	16
38.4 K	46	00	2E
19.2 K	94	00	5E
9600	190	00	BE
7200	254	00	FE
4800	382	01	7E
3600	510	01	FE
2400	766	02	FE
1800	1022	03	FE
1200	1534	05	FE
600	3070	OB	FE
300	6142	17	FE

Table 3-5. Typical Time Constraints for Asynchronous (x16) Clock

Baud Rate	Time Constant (Base 10)	WR13 Value (Hex)	WR12 Value (Hex)
19200	4	00	04
9600	IO	00	OA
7200	14	00	OE
4800	22	00	16
3600	30	00	1E
2400	46	00	2E
1800	62	00	3E
1200	94	00	5E
600	190	00	BE
300	382	01	7E
150	766	02	FE
75	1534	05	FE
50	2302	08	FE

3.5 SERIAL CHANNEL CLOCK CONFIGURATIONS

The receiver and/or transmitter can be independently programmed to accept their clock source from any of the following: the RXC/RT signal, the baud rate generator, or the digital phase locked loop (see the SCC manual). (TXC/TT may not be programmed as a clock source.) The receiver option is specified in WRl l:D6,D5, the transmitter in WRl l:D4, D3.

The TXC/TT output signal may be programmed to output any of the following: the baud rate generator, the digital phase lock loop, or the transmitter's clock. This is selected via WRl 1:D1,D0.

Any combination of clock rate and baud rate options may be used in synchronous or asynchronous modes. Four typical examples are given below:

1) Asynchronous Operation
The baud rate generator is used as the transmitter and receiver clocks. The master clock signal received on the pin PCLK is used for the generator's input. The external clock's RXC/RT and TXC/TT are not used.

2) Synchronous Operation. External Transmitter and Receiver Timing Definition
The RXC/RT clock input is used for the transmitter and receiver clocks. TXC/SD output will be synchronized to the clock input on RXC/RT. RXD/RT input will be sampled by clock input RXC/RT. The baud rate generator is not used.

3) Synchronous Operation. Internal Transmitter and Receiver Timing Definition
The baud rate generator is used for the transmitter and receiver clocks. TXC/TT output signal is programmed to output the baud rate generator. TXC/SD output will be synchronized to the clock output TXC/TT. RXD/RD input will be sampled by clock output TXC/TT.

4) Synchronous Operation. External Receiver Timing Definition and Internal Transmitter Timing Definition
The baud rate generator is used for the transmitter clock and is sent out on the TXC/TT line. The RXC/RT signal is used for the receiver clock. TXD/SD output will be synchronized to the clock output TXC/TT. RXD/RD input will be sampled by clock input RXC/RT.

3.6 MODULE RESET OPERATION

The module is reset by the assertion of VMEbus signal SYSRESET*. In response, the module will reset its VMEbus interface and the SCCs. Refer to the SCC technical manual for SCC reset operation.

3.7 GENERAL PROGRAMMING CONSIDERATIONS

This section outlines programming rules which apply to all modes of operation. These constraints are dictated by hardware configurations.

WRl - Set D7, D6, D5 to 0, 1, 0. This will disable the DMA and WAIT features of the SCCs. Polled or interrupt operation must be used.

WR4- D5, D4 must not be programmed for external sync modes of operation.

WR9- Set Dl to 0. This will enable the interrupt vector feature of the SCC. There are no other sources of IACK vectors on the module.

WRll- Set D7 to 0. This will disable the external crystal oscillator feature of the SCC. The SCC pin /TRXC must not be programmed as a clock source for the receiver (D6,D5) or the transmitter (D4,D3). Set D2 to 1 to select the /TRXC pin as an output.

WR14 - Set D2 to 0 to program the DTR/REQ pin to the DTR function.

3.7.1 Asynchronous Operation Initialization

This section describes the steps required to set up the SCCs for asynchronous operation. These steps apply to any channel and should be followed in the specified order.

1) Issue the Channel Reset command (WR9:D7,6).

2) Set WR4 as follows clock mode in D7,D6 (16X is suggested); number of stop bits in D3,D2; and parity odd/even/enable in Dl, DO.

3) Set WR3 as follows: number of receive bits/character in D7,D6; auto enables as required in D5; receiver disable DO=O.

4) Set WR5 as follows: state of DTR and CTS in D7, Dl; number of transmit bits/character in D6,D5; transmitter disable D3=0.

5) Set WRl0 for NRZ D6,D5=0,0.

6) Set interrupt or polled operation (refer to Section 3.3).

7) Set clocking options (refer to Section 3.4).

8) Enable receiver (WR:DO) and transmitter (WR5:D3) as required.

3.7.2 Synchronous Operation Initialization

This section describes the steps required to set up the SCCs for synchronous operation. These steps apply to any channel and should be followed in the specified order.

1) Issue the Channel Reset command (WR9:D7,6).

2) Set WR4 as follows: X.1 clock mode D7,D6=0,0; type of sync D5,D4; sync mode enabled D3,D2=0,0; parity odd/even/enable in D1,DO.

3) Set WRI0 as required.

4) Set WR6 and WR7 to the sync character or SDLC address as required.

5) Set WR3 as follows: number of receive bits/character in D7,D6; D5,D4,D3,D2,D 1 as required; receiver disabled DO=O.

6) Set WR5 as follows: state of DTR and CTS in D7,Dl; number of transmit bits/character in D6,D5; D4,D2,D0 as required; and transmitter disabled D3=0.

7) Set WR14 as required.

8) Set interrupt or polled operation (refer to Section 3.3).

9) Set clocking options (refer to Section 3.4).

10) Enable receiver (WR3:DO) and transmitter (WR5:D3) as required.

3.8 PROGRAMMING EXAMPLE

```
*****************************************************************************
*
*                    XVME-400/40 l/490/49 1 Sample Program
*
*                    Polled mode - Asynchronous Operation
*
*****************************************************************************

*****************************************************************************
*
*                                  EQUATES
*
*****************************************************************************

BASE
EQU       $00FF0000              * Base address of module
STACK     EQU       $A00         * Start of stack
SCCIAC    EQU       BASE+13      * SCC #l control register

          ORG       $800000

START
          M0VEA.L   #STACK,A7    * Load stack pointer
          M0VE.W    #$2000,SR    * Load status register

* Configure cha nnel A of SCC #I

          LEA.L     SCCIAC,AO    * Load address of module
          M0VE.W    #$000A,D7    * 9600 baud time constant
          BSR.S     ASYNC_INIT   * Initialize channel A

* Read a character from channel A of SCC #l

LOOP      LEA.L     SCCIAC,A3    * Load address of SCC control reg.
          BSR       RPOLA        * Get a character

* Write a charac ter to channel A of SCC #l

          LEA.L     SCC 1 AC,A2  * Load address of SCC control reg.
          BSR       TPOLA        * Echo the character

          BSR.S     LOOP
```

```
*******************************************************************************
*
*       This subroutine will initialize the specified SCC channel for asynchronous
*       operation.
*
*       On entry:
*             A0.L  = SCC control register address
*             D7.W = [ WR13 | WR12 ] baud rate time constant
*
*       On exit:
*
*             Transmitter and receiver enabled
*******************************************************************************


ASYNC_INIT:
        M0VE.B    #9,(A0)              * Set WR9
        M0VE.B    #$80,(AO)            * Reset channe l A, SCC #l
        M0VE.B    #4,(A0)              * Set WR4: X16 clock, l stop bit
        M0VE.B    #%01000101,(A0)      *  Odd parity enabled

        M0VE.B    #3,(A0)              * Set WR3: 8 RX bits disabled
        M0VE.B    #%11000000,(A0)      * No auto enable

        M0VE.B    #5,(A0)              * Set WR5: DTR and RTS asserted
        M0VE.B    #%ll lOOOlO,(AO)     * 8 TX bits, TX disabled

        M0VE.B    #l,(AO)              * Set WRl: DMA/WAIT pins
        M0VE.B    #%01000100,(A0)      * Set RX,TX, ext. int. disabled
                                       *  Parity = special condition

        M0VE.B    #2,(A0)              * Set WR2
        M0VE.B    #$4O,(AO)            * IACK vector = $40

        M0VE.B    #9,(A0)              * Set WR9: status lo w, MIE set
        M0VE.B    #%00001001,(A0)      * DLC=O¦ IACK vector variable

        M0VE.B    #1O,(AO)             * Set WRl0 to NRZ
        M0VE.B    #0,(AO)

        M0VE.B    #1l,(AO)             * Set WRll: no XTAL
        M0VE.B    #%0l0l0ll0,(A0)      *  RX TX clock=BRG
                                       * TRXC=BRG

        R0R.W     #8,D7                * Set WR13: High order
        M0VE.B    #13,(AO)             *  Time constant
        M0VE.B    D7,(AO)
```

```
R0L.W     #8,D7          * Set WR12: Low order
M0VE.B    #12,(AO)       * Time constant
M0VE.B    D7,(AO)
M0VE.B    #14,(AO)       * Set WR14
M0VE.B    #2,(AO)        * BRG source=PCLK
M0VE.B    #14,(AO)
M0VE.B    #3,(A0)        * Enable BRG

M0VE.B    #15,(AO)       * Set WR15: Disable all external
M0VE.B    #0,(A0)        * interrupts

M0VE.B    #3,(A0)        * Enable receiver
M0VE.B    #%11000001,(A0)

M0VE.B    #5,(AO)        * Enable transmitter
M0VE.B    #%l1101010,(A0)

RTS
```

```
*******************************************************************************
*
*   This routine will transmit a byte in polled mode.
*
*
*         On entry:
*              A2 contains the address of the command
*              register of the SCC channel used for
*              transmitting.
*
*
*              D2.B contains the byte to be transmitted.
*
*******************************************************************************

TPOLA
          MOVEML  DO/D 1 /A 1  ,-(SP)    * Save registers
TXPOLL    M0VE.B  (A2),DO                * Read the contents of RR0
          BTST    #2,DO                  * Is TX buffer empty?
          BEQ.S   TXPOLL                 * No, then poll again
TXBFE     M0VE.B  D3,2(A2)               * Yes, move character to transmit
                                         * data register

TXIT      MOVEML  (SP)+,DO/Dl /A 1       * Restore registers
          RTS
```

```
*******************************************************************************
*
*
*       This routine will receive a byte of data in polled mode.
*
*
*           On entry:
*
*                   A3 contains the address of the command
*                   register of the SCC channel used for
*                   receiving.
*
*           On exit:
*
*                   D3.B contains the byte which was received.
*
*******************************************************************************

RPOLA
            M0VE M.L  DO/D 1 /A 1 ,-(SP)    * Save registers
RXPOLL      M0VE.B  (A3),DO                 * Read the contents of RR0
            BTST      #O,DO                 * Is a character available?
            BEQ.S     RXPOLL                * No, then try again
RXCHA       M0VE.B  2(A3),D3                * Get the character

RXIT        MOVEM.L (SP)+,D0/D  1 /A1       * Restore registers
            RTS

            END
```

```
**************************************************************************
*
*   This routine will initialize the specified SCC channel to asynchronous
*   operation.  A hardware reset is assumed before code is executed.
*
*   IN:  A0.1 = SCC Control Register Address
*        D7.W = [ WR13 |WR12 ] Baud Rate Time Constant
*
*   OUT:          Transmitter and receiver enabled.
*                 All channel interrupts disabled.
*                 IACK Vector Register set to $40, MIE bit set, DLC bit reset.
*                 Variable IACK Vector enabled, low status
*                 Xl6 Clock mode, 1 stop bit, odd parity enabled
*                 Transmitter and receiver set to 8 bits/character
*                 No auto enables
*                 DTR/TR and RTS/RS asserted
*                 Receive clock, transmit clock, and TXC/TT programed for
*                 BRG Output
*                 BRG clock = PCLK
*
**************************************************************************

ASYNC-INIT:

        M0VE.B  #4,(A0)             * Set WR4: Xl6 clock, 1 stop bit
        M0VE.B  #%01000101,(A0)     * Odd parity enabled

        M0VE.B  #3,(A0)             * Set WR3: 8 RX bits
        M0VE.B  #$l 1 000000,(A0)   * No auto enable, RX disabled

        M0VE.B  #5,(A0)             * Set WR5: DTR & RTS asserted,
        M0VE.B  #%11l0001l0,(A0)    * 8 TX bits, TX disabled

        M0VE.B  #1,(A0)             *: Set WRI: DMA/WAIT pins,
        M0VE.B  #%01000100,(A0)     *: RX, TX, EXT INT disabled,
                                    *: Parity = Special condition

        M0VE.B  #2,(A0)             *: WR2
        M0VE.B  #$40,(A0)           * IACK Vector = $40

        M0VE.B  #9,(A0)             * Set WR9: Status Low, MIE set,
        M0VE.B  #%00001001,(A0)     * DLC=O, IACK Vector variable

        M0VE.B  #l0,(A0)            * Set WRl0 to NRZ
        M0VE.B  #l0,(A0)

        M0VE.B  #l l,(A0)           lt Set WRll: No XTAL,
        M0VE.B  #%0l0l0l  l0,(A0)   * RX, TX Clock = BRG,
                                    * TRXC = BRG
```

```
R0R.W    #8,D7          * Set WR13 = High order
M0VE.B   #13,           * Time constant
M0VE.B   D7,(AO)

R0L.W    #8,D7          * Set WR12 = Low Order
M0VE.B   #12,(AO)       * Time constant
M0VE.B   D7,(AO)

M0VE.B   #14,(A0)       * Set WR14:
M0VE.B   #2,(A0)        * BRG source = PCLK
M0VE.B   #14,(A0)
M0VE.B   #3,(A0)        * Enable BRG

M0VE.B   #15,(A0)       * Set WR15: Disable all external
M0VE.B   #0,(A0)        * Interrupts

M0VE.B   #3,(A0)        * Enable receiver
M0VE.B   #%11000001,(A0)

M0VE.B   #5,(A0)        * Enable transmitter
M0VE.B   #%11l0l0l0,(A0)

RTS
```

Appendix A

VMEbus CONNECTOR/PIN DESCRIPTIONS

Pl BACKPLANE CONNECTOR

All the modules have the rear-edge connector PI, which is a 96-pin bus connector consisting of three rows of 32 pins each. (Row A is physically closest to the board. See Table A-2). The signals carried by connector Pl are the standard address, data, and control signals required for a Pl backplane interface as defined by the VMEbus specification. Table A-l identifies and defines the signals carried by the Pl connector.

Table A-l. PI - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	lB:3	AC FAILURE: Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	lA:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1 A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 1B:16,17, 18,19 1C:14	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*		ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.

Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A0I-A23	1A:24-30 lC:15-30	ADDRESS BUS (bits l-23): Three-state driven address lines that specify a memory address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.
BBSY*	1B:l	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	IB:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:ll	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*- BG3IN*	1B:4,6, 8,l0	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*- BG3OUT*	lB:5,7, 9,ll	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.

Table A-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BR0*-BR3*	lB:12-15	BUS REQUEST (0-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	IA:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data buss lines (D00-D07).
DSl*	IA:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D0-D15).
DTACK*	lA:16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	lA:l-8 lC:l-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	lA:9,11, 15,17,19, 1B:20,23, lC:9 2B:2,12, 22,31	GROUND

Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
IACK*	1A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot **1** IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQl*-IRQ7*	1B:24-30	INTERRUPT REQUEST (1-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	lC:l3	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERV-ED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	lB:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized,
SERDAT	1B:22	A reserved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	1A:l0	SYSTEM CLOCK: **A** constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.

Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSFAIL*	1C:l0	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	lC:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	lA:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or write. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	lB:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5v	1A:32 lB:32 1C:32 2B:l,l3,32	+5 VDC POWER: Used by system logic circuits.
+12v	lC:31	+12 VDC POWER: Used by system logic circuits.
-12v	lA:31	-12 VDC POWER: Used by system logic circuits.

Table A-2. Pl Signal Identification

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	DO8
2	DO1	BCLR*	DO9
3	DO2	ACFAIL*	Dl0
4	DO3	BG0IN*	Dll
5	DO4	BGOOUT*	D12
6	DO5	BGlIN*	D13
7	DO6	BGlOUT"	D14
8	DO7	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG30UT*	BERR*
12	DSl*	BR0*	SYSRESET*
13	DSO*	BRl*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
I8	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5"	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQl*	A08
31	-12v	+5V STDBY	+12v
32	+5v	+5v	+5v

BACKPLANE CONNECTOR P2

The **XVME-490** and XVME-491 have the rear-edge connector P2, which is a 96-pin bus connector consisting of three rows of 32 pins each. (Row A is physically closest to the board.) Table A-3 identifies the RS-232C P2 signals for the XVME-490, while Table A-4 shows the RS-485/422A signals for the XVME-491.

Table A-3. P2 Signal Identification for XVME-490

Pin #	Row A Signal	Row B Signal	Row C Signal
1	TXDO	v c c	GND
2	RXDO	GND	GND
3	RTSO	NC	GND
4	RXCO Ch. 0	NC	GND
5	CTSO	NC	GND
6	DTRO	NC	GND
7	DCDO	NC	GND
8	TXCO	NC	GND
9	TXDl	NC	GND
10	RXDl	NC	GND
11	RTSl	NC	GND
12	RXCl Ch.1	GND	GND
13	CTSI	v c c	GND
14	DTR 1	NC	GND
15	DCDl	NC	GND
16	TXCl	NC	GND
17	TXD2	NC	GND
18	RXD2	NC	GND
19	RTS2	NC	GND
20	RXC2 Ch. 2	NC	GND
21	CTS2	NC	GND
22	DTR2	GND	GND
23	DCD2 .	NC	GND
24	TXC2	NC	GND
25	TXD3	NC	GND
26	RXD3	NC	GND
27	RTS3	NC	GND
28	RXC3 Ch. 3	NC	GND
29	CTS3	NC	GND
30	DTR3	NC	GND
31	DCD3	GND	GND
32	TXC3	v c c	GND

NOTE

All P2 signal names are in the form "XXXN" where "N" is the serial channel number and "XXX" is the signal name. Signals with the same "XXX" function identically with respect to the particular channel.

Table A-4. P2 Signal Identification for the XVME-491

Pin #	Row A Signal	Row B Signal	Row C Signal
1	TXDO+	v c c	TXDO-
2	TXCO+	GND	TXCO-
3	RTSO+	NC	RTSO-
4	RXDO+ Ch. 0	NC	RXDO-
5	RXCO+	NC	RXCO-
6	CTSO+	NC	CTSO-
7	DCDO+	NC	DCDO-
8	GND	NC	GND
9	TXDl+	NC	TXDl-
10	TXCl+	NC	TXCl-
11	RTSl+	NC	RTSI-
12	RXDl+ Ch. 1	GND	RXDl-
13	RXCl+	v c c	RXCl-
14	CTSl+	NC	CTSl-
15	DCDl+	NC	DCDl-
16	GND	NC	GND
17	TXD2+	NC	TXD2-
18	TXC2+	NC	TXC2-
19	RTS2+	NC	RTS2-
20	RXD2+ Ch. 2	NC	RXD2-
21	RXC2+	NC	RXC2-
22	CTS2+	GND	CTS2-
23	DCD2+	NC	DCD2-
24	GND	NC	GND
25	TXD3+	NC	TXD3-
26	TXC3+	NC	TXC3-
27	RTS3+	NC	RTS3-
28	RXD3+ Ch. 3	NC	RXD3-
29	RXC3+	NC	RXC3-
30	CTS3+	NC	CTS3-
31	DCD3+	GND	DCD3-
32	GND	v c c	GND

NOTE

All XVME-401 signal names are in the form "XXNZ", where "N" is the channel number, "Z" is + or - based on which half of the signal it is, and "XX" is the name of the signal.

JKl AND JK2 CONNECTORS

The XVME-400 and XVME-401 have JKl and JK2 connectors, which are 50-pin connectors consisting of three rows of 32 pins each. Table A-5 identifies the RS-232C signals carried by the JKl and JK2 connectors on the XVME-400. Table A-6 shows the RS-485/422A signals carried by the JKl and JK2 connectors on the XVME-401.

Table A-5. JKl and JK2 Signal Identification for XVME-400 (RS232C)

Pin Number	JKI Signal	JK2 Signal	Signal	Direction
3	TXDO	TXDl	Transmit Data	OUT
5	RXDO	RXDl	Receive Data	IN
7	RTSO	RTSl	Request To Send	OUT
8	RXCO Ch. 0	RXCl Ch. 1	Receiving Clock	IN
9	CTSO	CTSI	Clear To Send	IN
13	GND	GND	Ground	
14	DRTO	DTRl	Data Terminal Ready	OUT
15	DCDO	DCDl	Data Carrier Detected	IN
22	TXCO	TXCl	Transmitting Clock	OUT
28	TXD2	TXD3	Transmit Data	OUT
30	RXD2	RXD3	Receive Data	IN
32	RTS2	RTS3	Request To Send	OUT
33	RXC2 Ch. 2	RXC3 Ch. 3	Receiving Clock	IN
34	CTS2	CTS3	Clear To Send	IN
38	GND	GND	Ground	
39	DTR2	DTR3	Data Terminal Ready	OUT
40	DCD2	DCD3	Data Carrier Detected	IN
47	TXC2	TXC3	Transmitting Clock	OUT

NOTE

All XVME-400 signal names are in the form XXXN where "N" is the serial channel number and "XXX" is the name of the signal.

All JKl and JK2 pin numbers not referenced are not connected.

The pinouts of JKI and JK2 allow a 50-conductor flat cable to be connected, split into two 25-conductor sections, and have 25-pin D-type connectors installed on the two 25-conductor sections. The position of the signals relevant to the 25-pin D-type connectors will be in accordance with the RS-232C definition (no line Transitions are required):

TXD Pin 2
RXD Pin 3
RTS Pin 4
CTS Pin 5
GND Pin 7
DCD Pin 8
RXC Pin 17
DTR Pin 20
TXC Pin 24

Table A-6. JKl and JK2 Signal Identification for the XVME-401 (RS-485/422A)

Pin Number	JKl Signal	JK2 Signal	Signal	Direction
1	SDOB	SDlB	Transmit Data	OUT
2	SDOA	SDIA	Transmit Data	OUT
5	RDOB	RDlB	Receive Data	IN
6	RDOA	RDlA	Receive Data	IN
7	RSOB	RSlB	Request To Send	OUT
8	RSOA	RSlA	Request To Send	OUT
9	RTOB	RTlB	Receive Clock	IN
10	RTOA Ch. 0	RTIA Ch. 1	Receive Clock	IN
11	CSOB	CSlB	Clear To Send	IN
12	CSOA	CSlA	Clear To Send	IN
16	TROB	TRlB	Data Terminal Ready	OUT
17	TROA	TRIA	Data Terminal Ready	OUT
18	RROB	RRIB	Data Carrier Detect	IN
19	RROA	RRlA	Data Carrier Detect	IN
20	TTOB	TTlB	Transmit Clock	OUT
21	TTOA	TTlA	Transmit Clock	OUT
24	SC0	SC1	Logic Ground	GND
25	SGO	SGl	Logic Ground	GND
26	SD2B	SD3B	Transmit Data	OUT
27	SD2A	SD3A	Transmit Data	OUT
30	RD2B	RD3B	Receive Data	IN
31	RD2A	RD3A	Receive Data	IN
32	RS2B	RS3B	Request To Send	OUT
33	RS2A	RS3A	Request To Send	OUT
34	RT2B	RT3B	Receive Clock	IN
35	RT2A	RT3A	Receive Clock	IN
36	CS2B Ch. 2	CS3B Ch. 3	Clear To Send	IN
37	CS2A	CS3A	Clear To Send	IN
41	TR2B	TR3B	Data Terminal Ready	OUT
42	TR2A	TR3A	Data Terminal Ready	OUT
43	RR2B	RR3B	Data Carrier Detect	IN
44	RR2A	RR3A	Data Carrier Detect	IN
45	TT2B	TT3B	Transmit Clock	OUT
46	TT2A	TT3A	Transmit Clock	OUT
47 (2)	+5v	+5v		OUT
49	SC2	SC3	Logic Ground	GND
50	SG2	SG3	Logic Ground	GND

NOTE

All XVME-40 1 signal names are in the form "XXNZ", where "N" is the channel number, "Z" is A or B based on the polarity of the differential signal (as define d by RS-485), and "XX" is the name of the signal.

All JKl and JK2 pin numbers not referenced are not connected.

Sources of JKl /JK2. or P2 Connector Output Signals (one set for each serial channel)

TXD/SD SCC output pin TXD drives a line driver. Driver output is sent to this pin.

RTS/RS SCC output pin RTS* drives a line driver. Driver output is sent to this pin.

TXC/TT SCC output pin TRXC drives a line driver. Driver output is sent to this pin.

DTR/TR SCC output pin DTR* drives a line driver. Driver output is sent to this pin.

Destinations of JK 1 /JK2. or P2 Connector Input Signals (one set for each serial channel)

RXD/RD This input pin is buffered by a line receiver and is driven to the SCC input pin RXD.

CTS/CS This input pin is buffered by a line receiver and is driven to the SCC input pin CTS*.

RXC/RT This input pin is buffered by a line receiver and is driven to the SCC input pin RTXC.

DCD/RR This input pin is buffered by a line receiver and is driven to the SCC input pin DCD*.

Appendix B

QUICK REFERENCE GUIDE

Table B-l. XVME-400 and XVME-490 Jumper List

Jumper	Use
Jl	Determines whether the module will respond to supervisory or supervisory and non-privileged short I/O VMEbus cycles (refer to Section 2.4.2 of this manual).
JAl0-JAI5	Select module base address on any one of the 64 1K boundaries within the short I/O address space (refer to Section 2.4.1 of this manual).
JAI-JA3	Select the VMEbus interrupt level for the module (refer to Section 2.4.3 of this manual).

Table B-2. XVME-401 and XVME-491 Jumper List

Jumper	Use
Jl and J2	Bring the +5V supply to front-edge connectors JKl and JK2, respectively (XVME-401 only; refer to Section 2.4.4).
J3-J6	Allows tri-stating of any of the channels (refer to Section 2.4.5).
J7	Determines whether the module will respond to supervisory or supervisory and non-privileged short I/O VMEbus cycles (refer to Section 2.4.2).
JAI0-JAI5	Select module base address on any one of the 64 IK boundaries within the short I/O address space (refer to Section 2.4.1).
JAI-JA3	Select the VMEbus interrupt level for the module (refer to Section 2.4.3).

Table B-3. Addressing Options

Jumper Jl (XVME-400/490), or J7 (XVME-401/491)	Address Modifier to which the XVME-400/40l/490/491 Module will respond
In	(2DH) Supervisory only
out	(2DH) Supervisory or (29H) Non-privileged

Table B-4. Interrupt Level Jumper Positions

JA3	JA2	JAI	Interrupt Level Selected
In	In	In	None, VMEbus Interrupter disabled
In	In	out	Level 1
In	out	In	Level 2
In	out	out	Level 3
out	In	In	Level 4
out	In	out	Level 5
out	out	In	Level 6
out	out	out	Level 7

Table B-5. +5V Jumpers (XVME-401 only)

Jumper	Use
Jl	If J1 is installed, +5V will be connected to JKl (pin 47). If Jl is removed, JKl-47 will float.
J2	If J2 is installed, +5V will be connected to JK2 (pin 47). If J2 is removed, JK2-47 will float.

Table B-6. VMEbus Base Address Options

Jumpers						VME Base Address in VME Short I/O Address Space
JA15	JA14	JA13	JA12	JAI1	JA10	
In	In	In	In	In	In	0000H
In	In	In	In	In	out	0400H
In	In	In	In	out	In	0800H
In	In	In	In	out	out	0C00H
In	In	In	out	In	In	1000H
In	In	In	out	In	out	1400H
In	In	In	out	out	In	1800H
In	In	In	out	out	out	1C00H
In	In	out	In	In	In	2000H
In	In	out	In	In	out	2400H
In	In	out	In	out	In	2800H
In	In	out	In	out	out	2C00H
In	In	out	out	In	In	3000H
In	In	out	out	In	out	3400H
In	In	out	out	out	In	3800H
In	In	out	out	out	out	3C00H
In	out	In	In	In	In	4000H
In	out	In	In	In	out	4400H
In	out	In	In	out	In	4800H
In	out	In	In	out	out	4C00H
In	out	In	out	In	In	5000H
In	out	In	out	In	out	5400H
In	out	In	out	out	In	5800H
In	out	In	out	out	out	5C00H
In	out	out	In	In	In	6000H
In	out	out	In	In	out	6400H
In	out	out	In	out	In	6800H
In	out	out	In	out	out	6C00H
In	out	out	out	In	In	7000H
In	out	out	out	In	out	7400H
In	out	out	out	out	In	7800H
In	out	out	out	out	out	7C00H
out	In	In	In	In	In	8000H
out	In	In	In	In	out	8400H
out	In	In	In	out	In	8800H
out	In	In	In	out	out	8C00H
out	In	In	out	In	In	9000H
out	In	In	out	In	out	9400H
out	In	In	out	out	In	9800H
out	In	In	out	out	out	9C00H
out	In	out	In	In	In	A000H
out	In	out	In	In	out	A400H

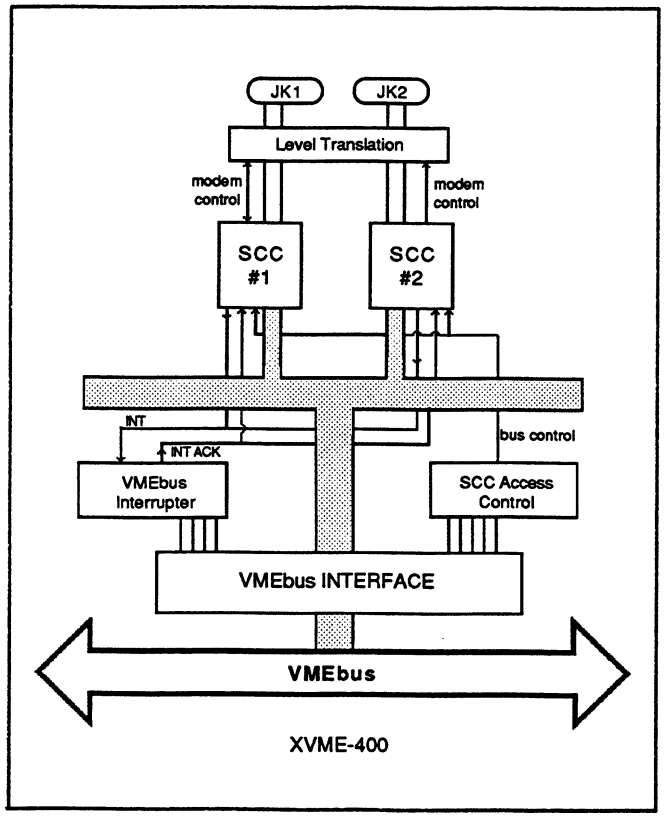
Table B-6. VMEbus Base Address Options (Cont'd)

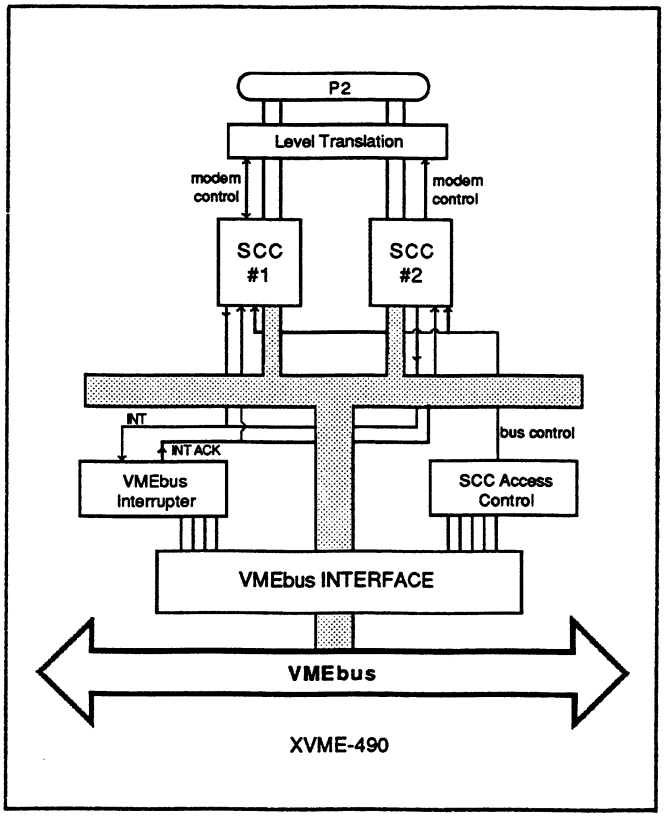
Jumpers						VME Base Address in VME Short I/O Address Space
JA15	JA14	JA13	JAI2	JAI1	JA10	
out	In	out	In	out	In	A800H
out	In	out	In	out	out	ACOOH
out	In	out	out	In	In	BOOOH
out	In	out	out	In	out	B400H
out	In	out	out	out	In	B800H
out	In	out	out	out	out	BCOOH
out	out	In	In	In	In	COOOH
out	out	In	In	In	out	C4OOH
out	out	In	In	out	In	C800H
out	out	In	In	out	out	CCOOH
out	out	In	out	In	In	DOOOH
out	out	In	out	In	out	D400H
out	out	In	out	out	In	D8OOH
out	out	In	out	out	out	DCOOH
out	out	out	In	In	In	EOOOH
out	out	out	In	In	out	E4OOH
out	out	out	In	out	In	E8OOH
out	out	out	In	out	out	ECOOH
out	out	out	out	In	In	FOOOH
out	out	out	out	In	out	F400H
out	out	out	out	out	In	F8OOH
out	out	out	out	out	out	FCOOH

Appendix C

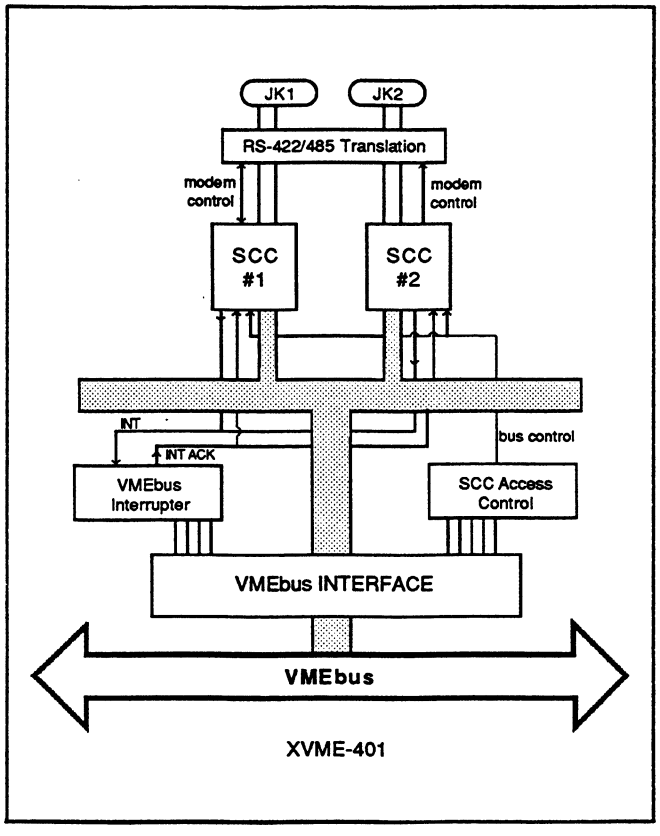
SCHEMATICS & DIAGRAMS

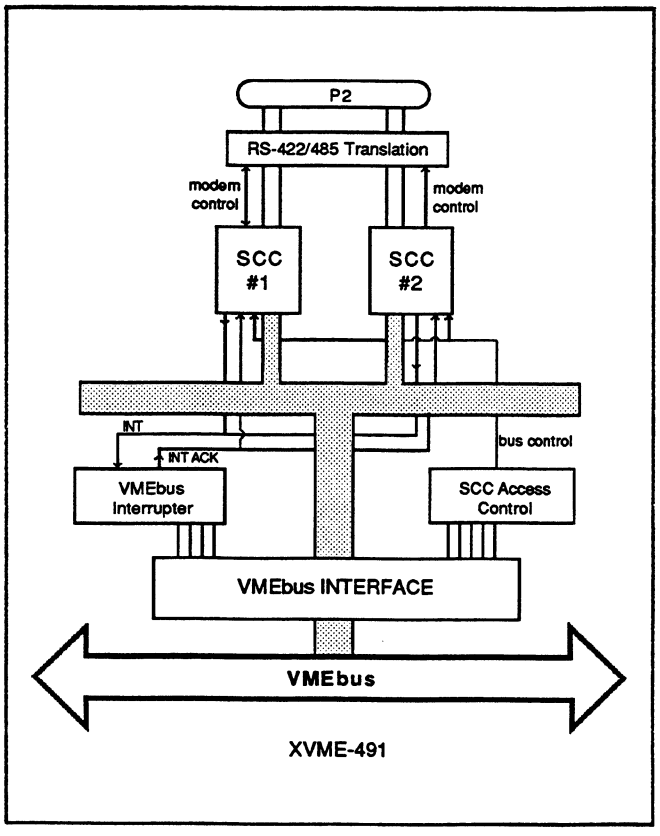
Block Diagram: XVME-400 and XVME-490



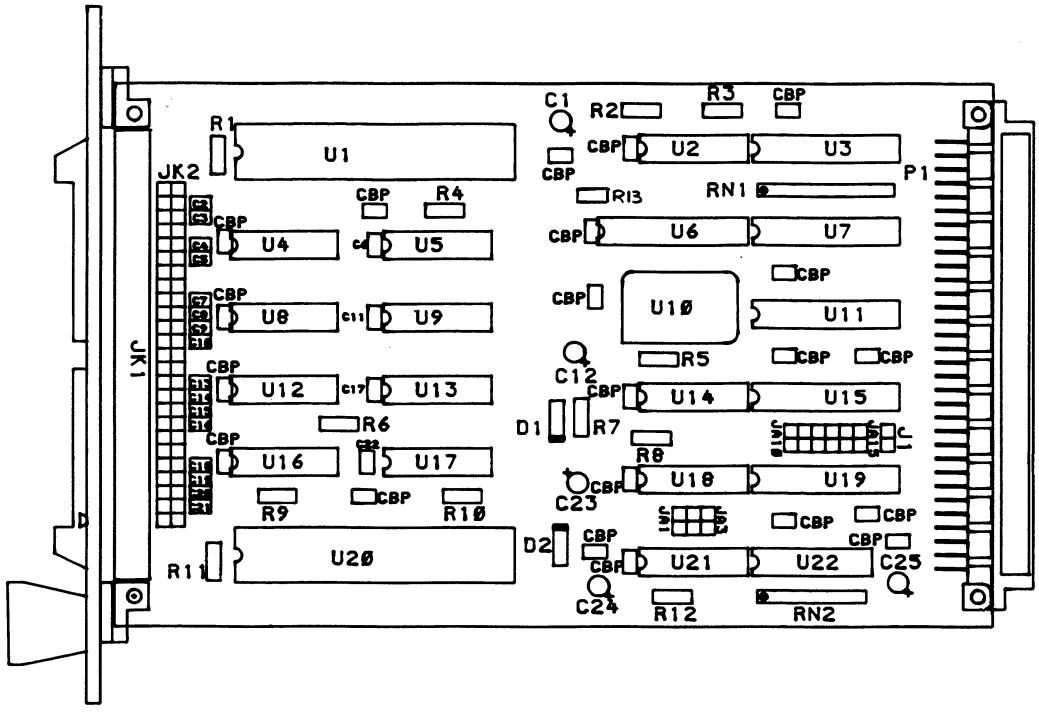


Block Diagram: XVME-401 and XVME-491

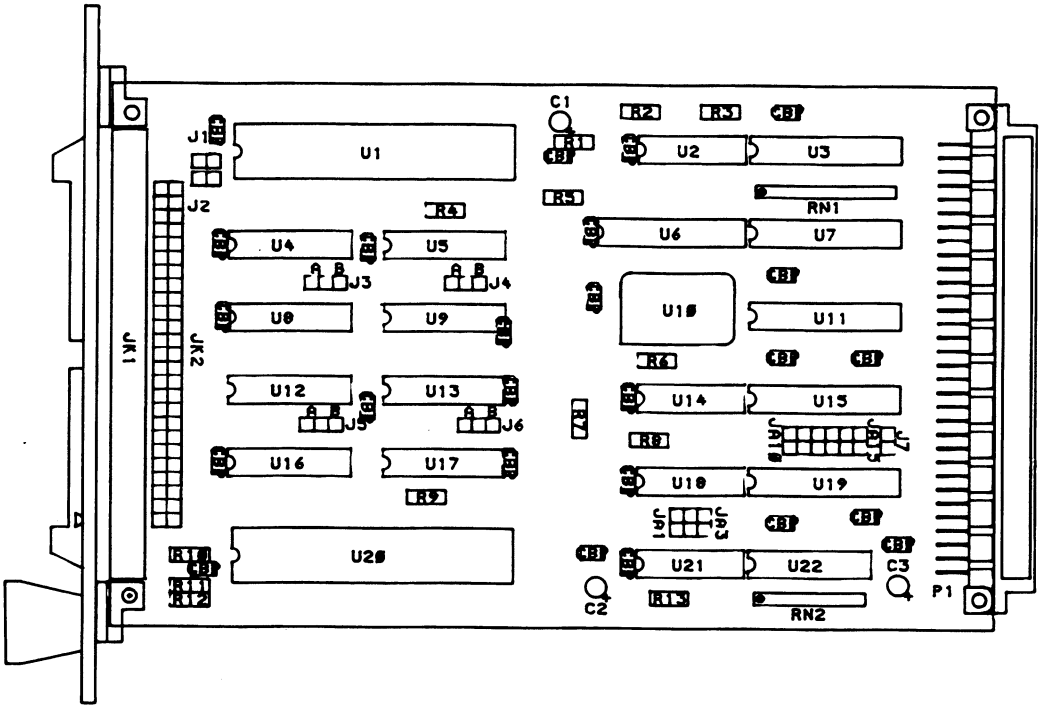




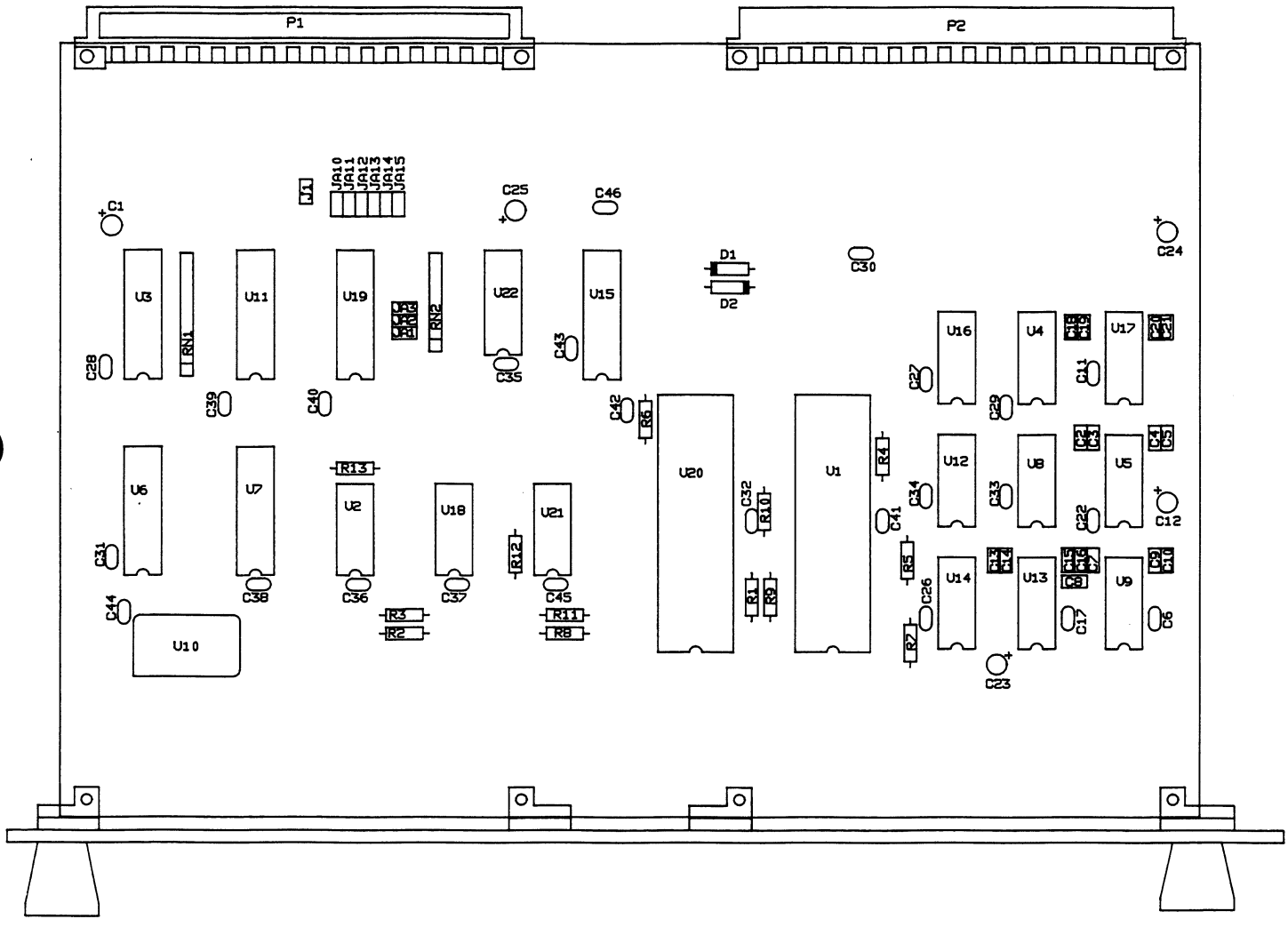
XVME-400 Assembly Drawing



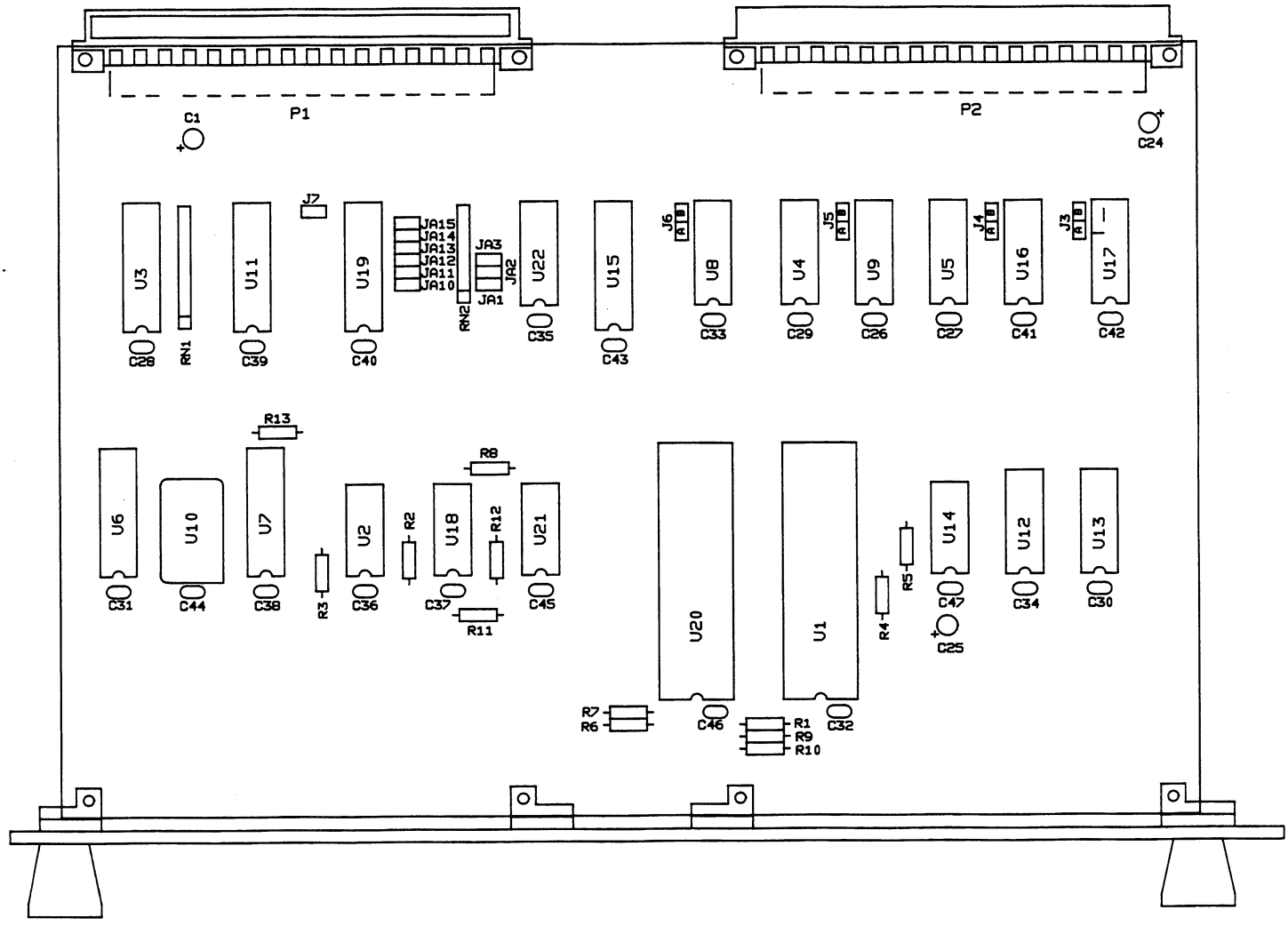
XVME-401 Assembly Drawing

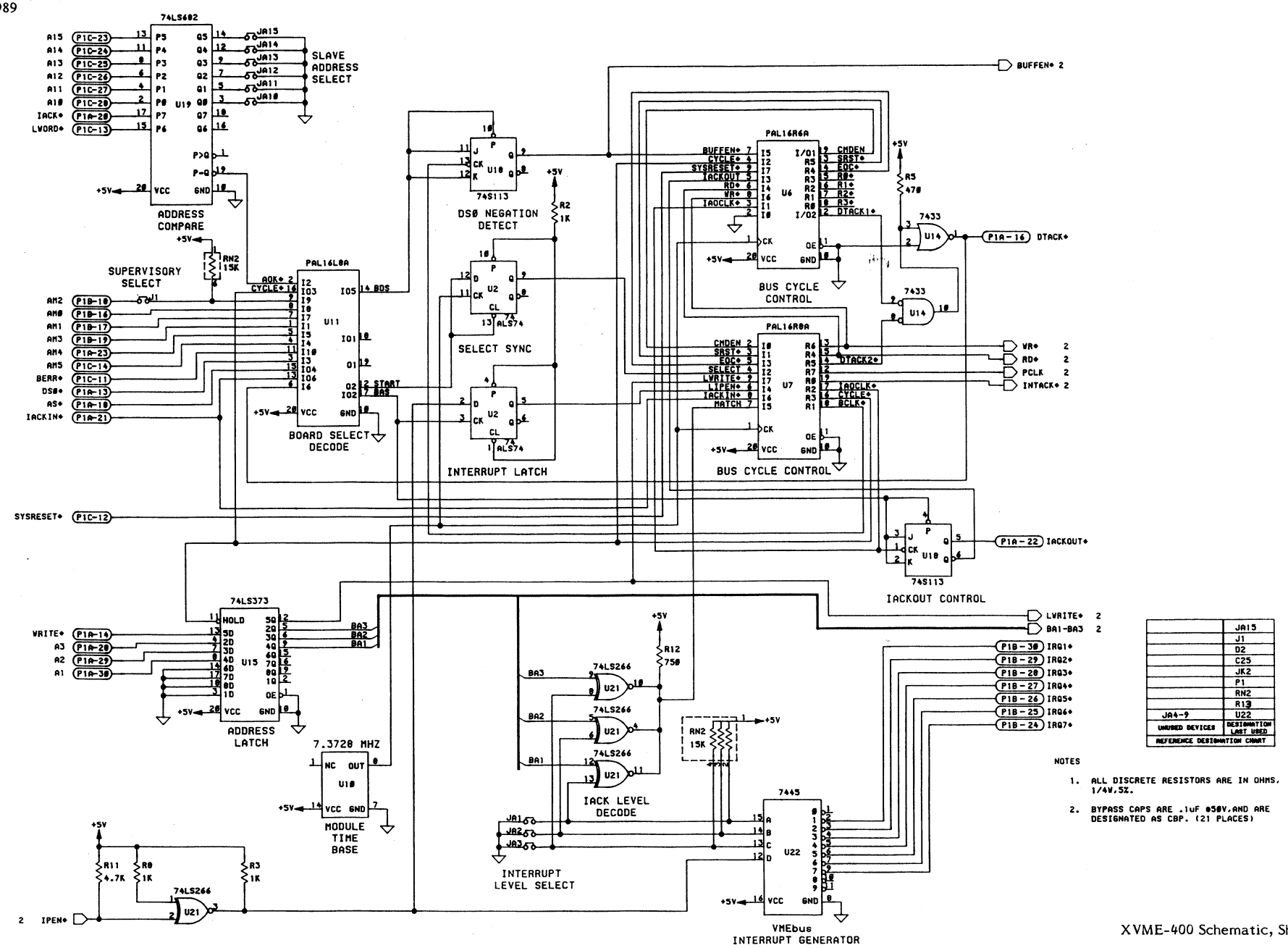


XVME-490 Assembly Drawing



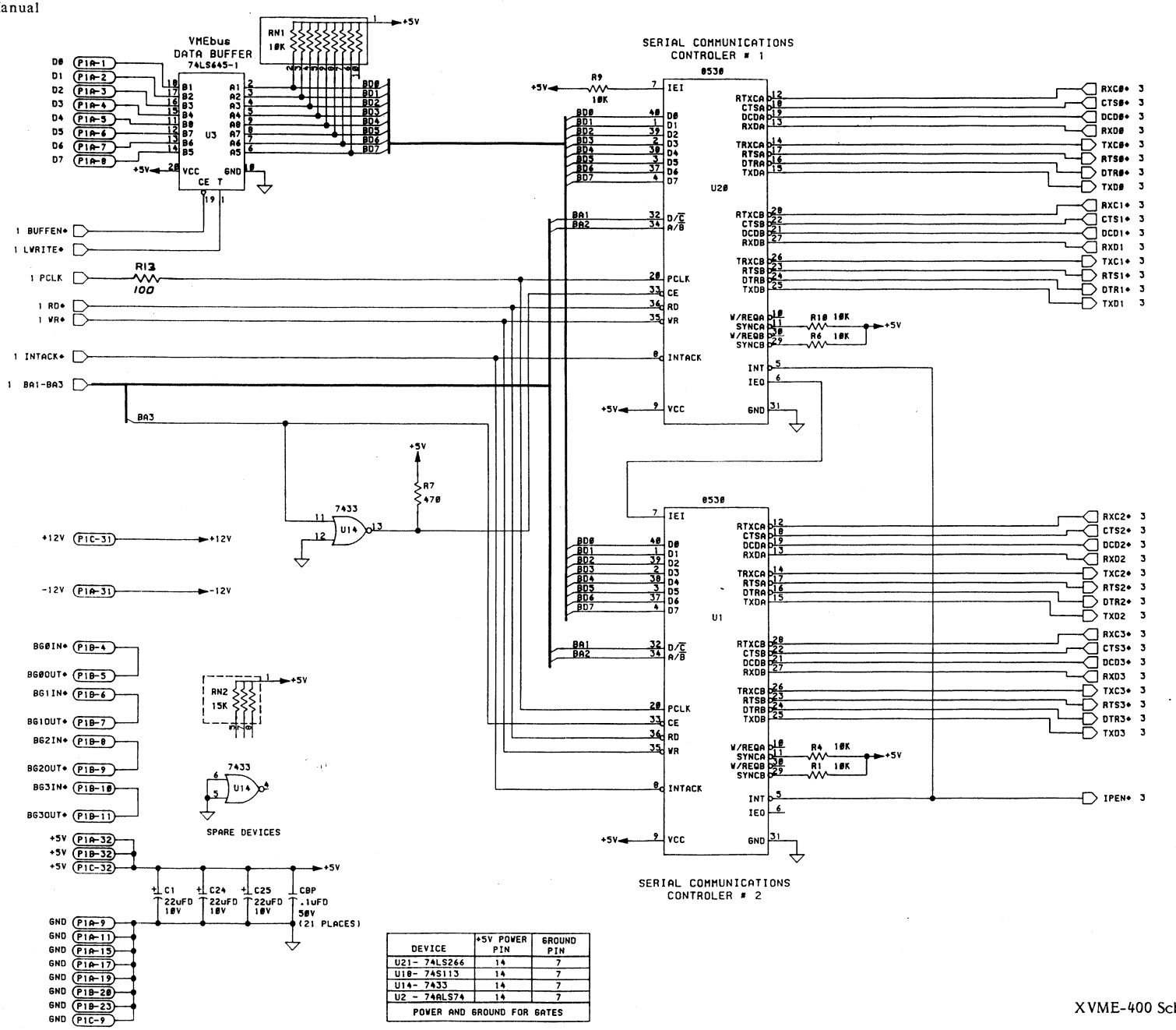
XVME-491 Assembly Drawing



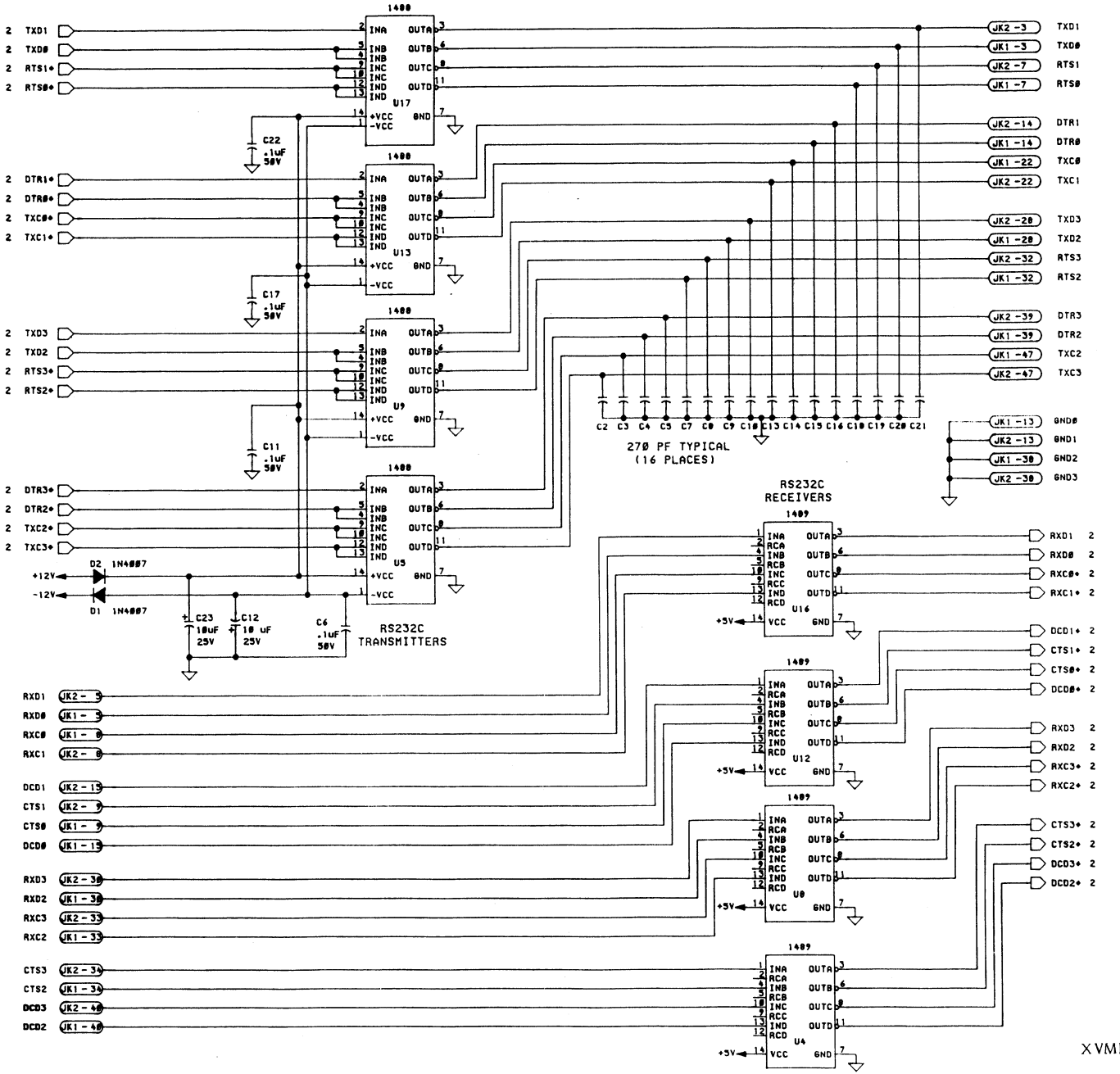


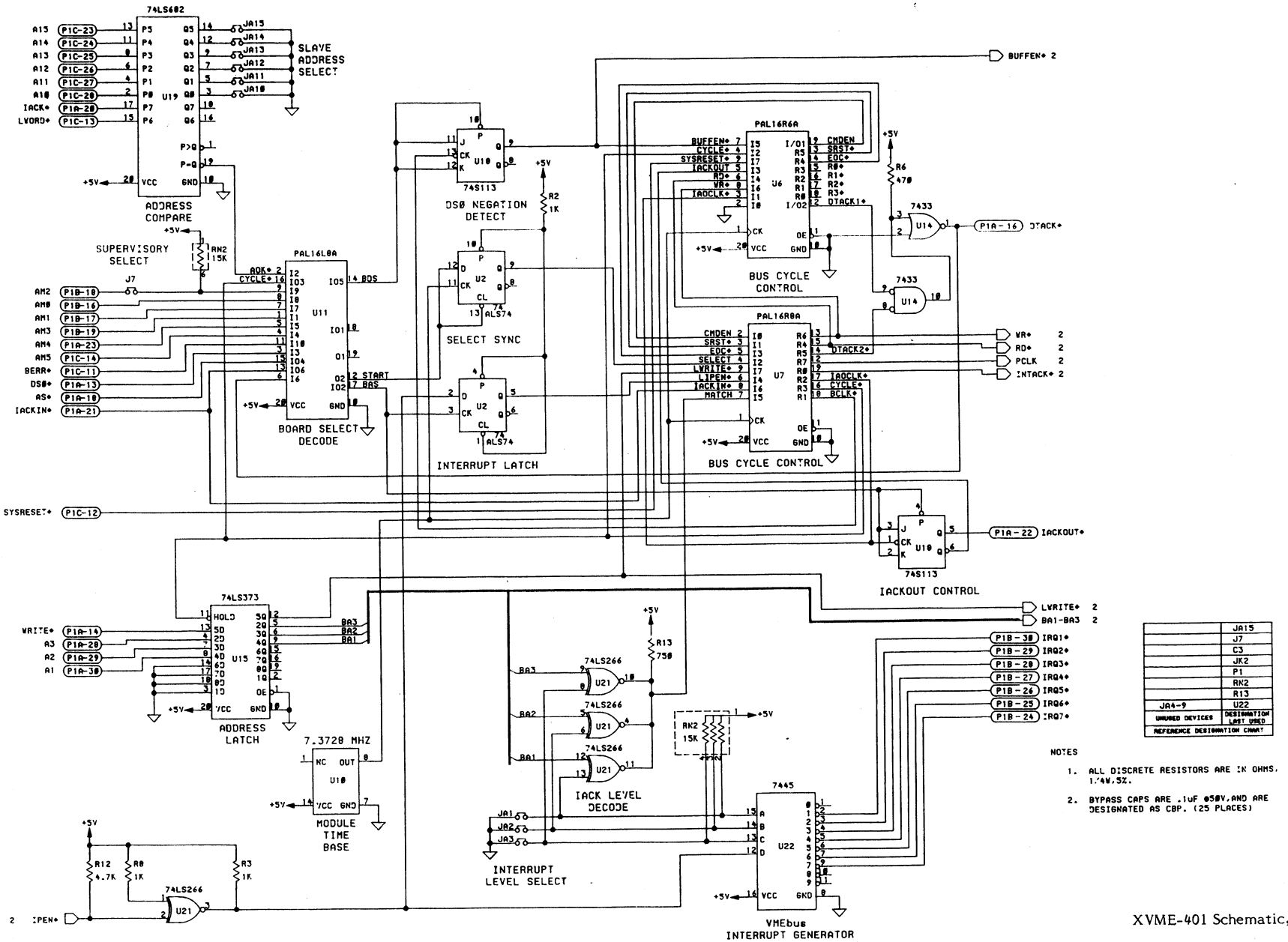
NOTES

1. ALL DISCRETE RESISTORS ARE IN OHMS, 1/4W,5%.
2. BYPASS CAPS ARE .1uF @50V.AND ARE DESIGNATED AS CBP. (21 PLACES)

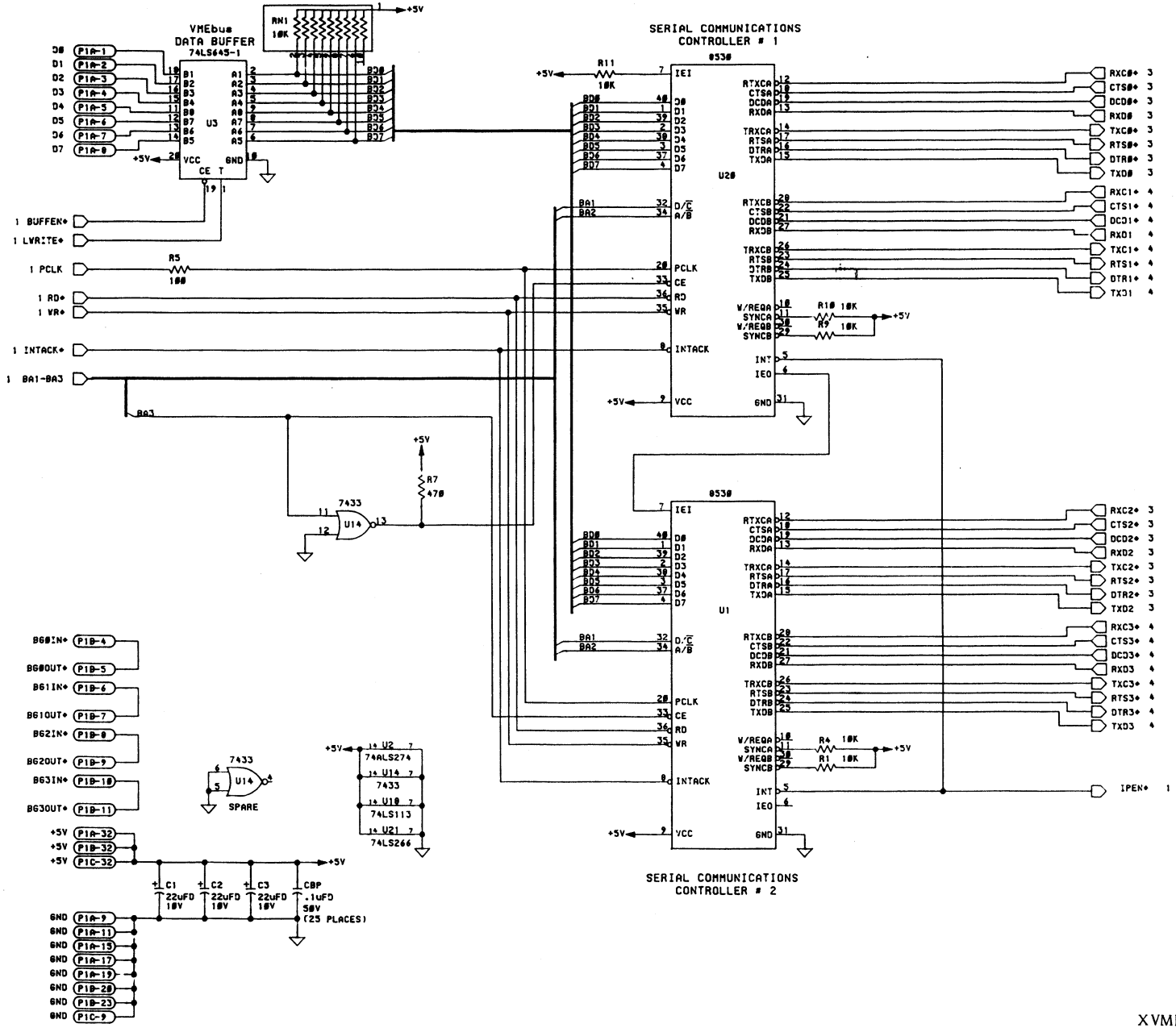


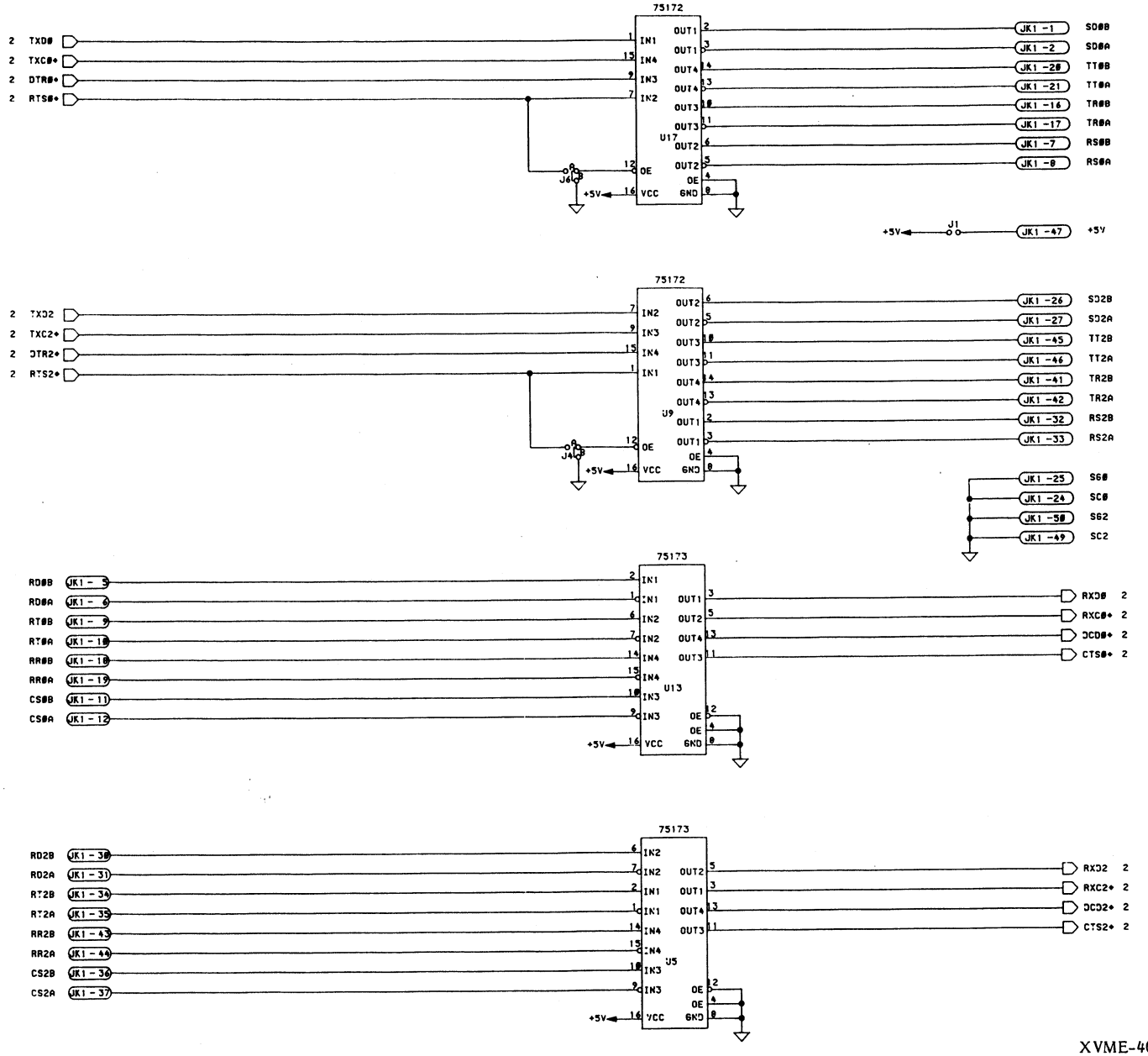
DEVICE	+5V POWER PIN	GROUND PIN
U21- 74LS266	14	7
U18- 74S113	14	7
U14- 7433	14	7
U2 - 74ALS74	14	7
POWER AND GROUND FOR GATES		


TXD1
TXD0
RTS1*
RTS0*
DTR1*
DTR0*
TXC0*
TXC1*
TXD3
TXD2
RTS3*
RTS2*
DTR3*
DTR2*
TXC2*
TXC3*
U17
U13
U9
U5
1488
+VCC
-VCC
GND
C22 .1uF 50V
C17 .1uF 50V
C11 .1uF 50V
D2 1N4007
D1 1N4007
+12V
-12V
C23 10uF 25V
C12 10 uF 25V
C6 .1uF 50V
RS232C TRANSMITTERS
JK2 -3 TXD1
JK1 -3 TXD0
JK2 -7 RTS1
JK1 -7 RTS0
JK2 -14 DTR1
JK1 -14 DTR0
JK1 -22 TXC0
JK2 -22 TXC1
JK2 -28 TXD3
JK1 -28 TXD2
JK2 -32 RTS3
JK1 -32 RTS2
JK2 -39 DTR3
JK1 -39 DTR2
JK1 -47 TXC2
JK2 -47 TXC3
C2 C3 C4 C5 C7 C8 C9 C10 C13 C14 C15 C16 C18 C19 C20 C21
270 PF TYPICAL
(16 PLACES)
JK1 -13 GND0
JK2 -13 GND1
JK1 -30 GND2
JK2 -30 GND3
RS232C RECEIVERS
1489
U16
U12
U8
U4
+5V
VCC
RXD1 2
RXD0 2
RXC0* 2
RXC1* 2
DCD1* 2
CTS1* 2
CTS0* 2
DCD0* 2
RXD3 2
RXD2 2
RXC3* 2
RXC2* 2
CTS3* 2
CTS2* 2
DCD3* 2
DCD2* 2
RXD1 JK2 - 5
RXD0 JK1 - 5
RXC0 JK1 - 8
RXC1 JK2 - 8
DCD1 JK2 - 15
CTS1 JK2 - 9
CTS0 JK1 - 9
DCD0 JK1 - 15
RXD3 JK2 - 30
RXD2 JK1 - 30
RXC3 JK2 - 33
RXC2 JK1 - 33
CTS3 JK2 - 34
CTS2 JK1 - 34
DCD3 JK2 - 40
DCD2 JK1 - 40

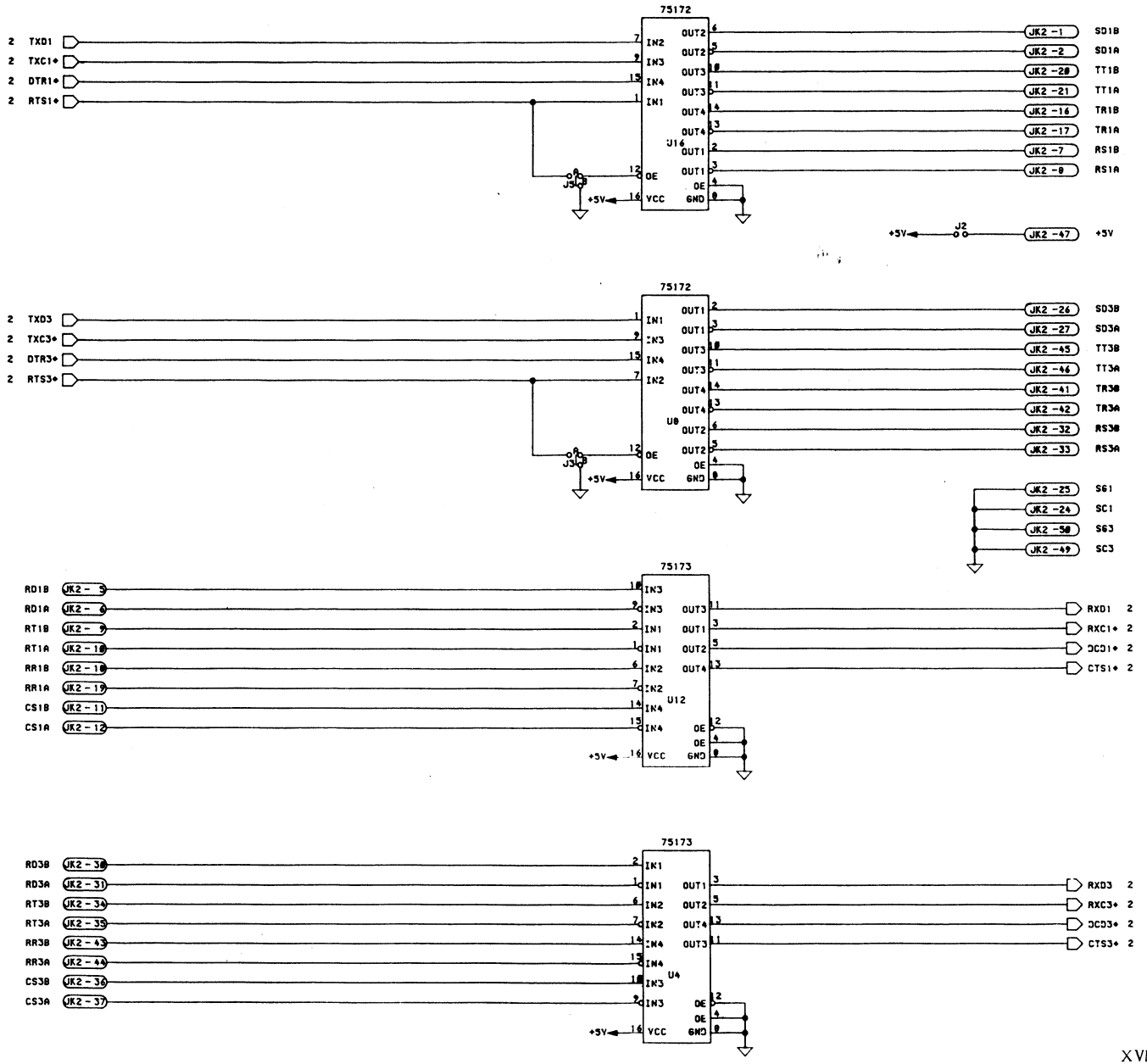


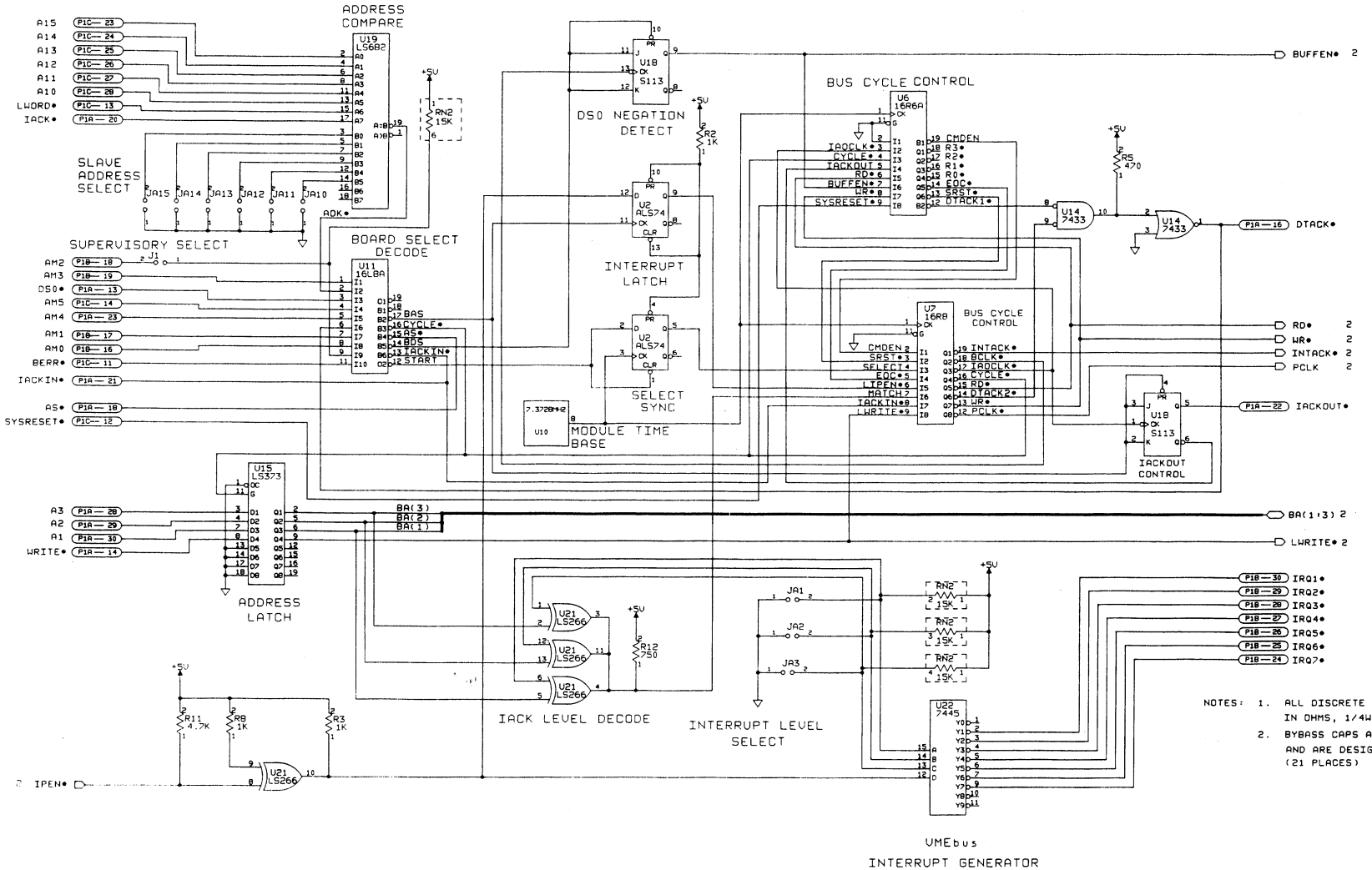
XVME-401 Schematic, Sheet 1 of 4


VMEbus
DATA BUFFER
74LS645-1
U3
RN1
10K
+5V
D0
D1
D2
D3
D4
D5
D6
D7
P1A-1
P1A-2
P1A-3
P1A-4
P1A-5
P1A-6
P1A-7
P1A-8
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
VCC
GND
CE
T
1 BUFFEN*
1 LWRITE*
1 PCLK
1 RD*
1 WR*
1 INTACK*
1 BA1-BA3
BA3
R5
180
R7
470
7433
U14
SERIAL COMMUNICATIONS
CONTROLLER # 1
8530
R11
10K
IEI
IEO
INT
INTACK
PCLK
CE
RD
WR
D/C
A/B
W/REQA
SYNCA
W/REQB
SYNCB
R10 10K
R9 10K
RTXCA
CTSA
DCDA
RXDA
TRXCA
RTSA
DTRA
TXDA
RTXCB
CTSB
DCDB
RXDB
TRXCB
RTSB
DTRB
TXDB
U28
U1
RXC0* 3
CTS0* 3
DCD0* 3
RXD0 3
TXC0* 3
RTS0* 3
DTR0* 3
TXD0 3
RXC1* 4
CTS1* 4
DCD1* 4
RXD1 4
TXC1* 4
RTS1* 4
DTR1* 4
TXD1 4
RXC2* 3
CTS2* 3
DCD2* 3
RXD2 3
TXC2* 3
RTS2* 3
DTR2* 3
TXD2 3
RXC3* 4
CTS3* 4
DCD3* 4
RXD3 4
TXC3* 4
RTS3* 4
DTR3* 4
TXD3 4
R4 10K
R1 10K
IPEN* 1
SERIAL COMMUNICATIONS
CONTROLLER # 2
B60IN*
B60OUT*
B61IN*
B61OUT*
B62IN*
B62OUT*
B63IN*
B63OUT*
P1B-4
P1B-5
P1B-6
P1B-7
P1B-8
P1B-9
P1B-10
P1B-11
SPARE
74ALS274
74LS113
74LS266
U2
U10
U21
P1A-32
P1B-32
P1C-32
C1
C2
C3
CBP
22uFD
10V
.1uFD
50V
(25 PLACES)
GND
P1A-9
P1A-11
P1A-15
P1A-17
P1A-19
P1B-20
P1B-23
P1C-9

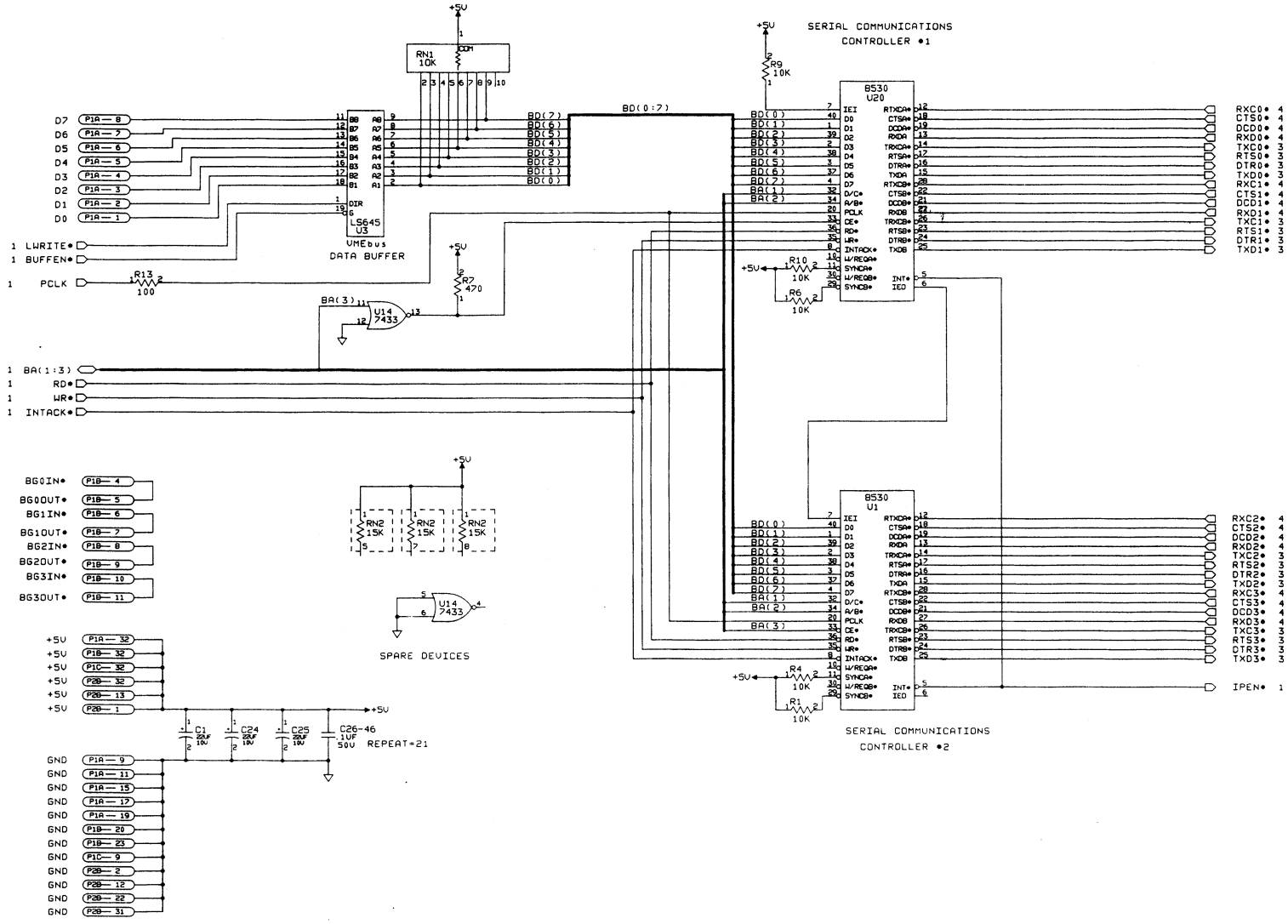


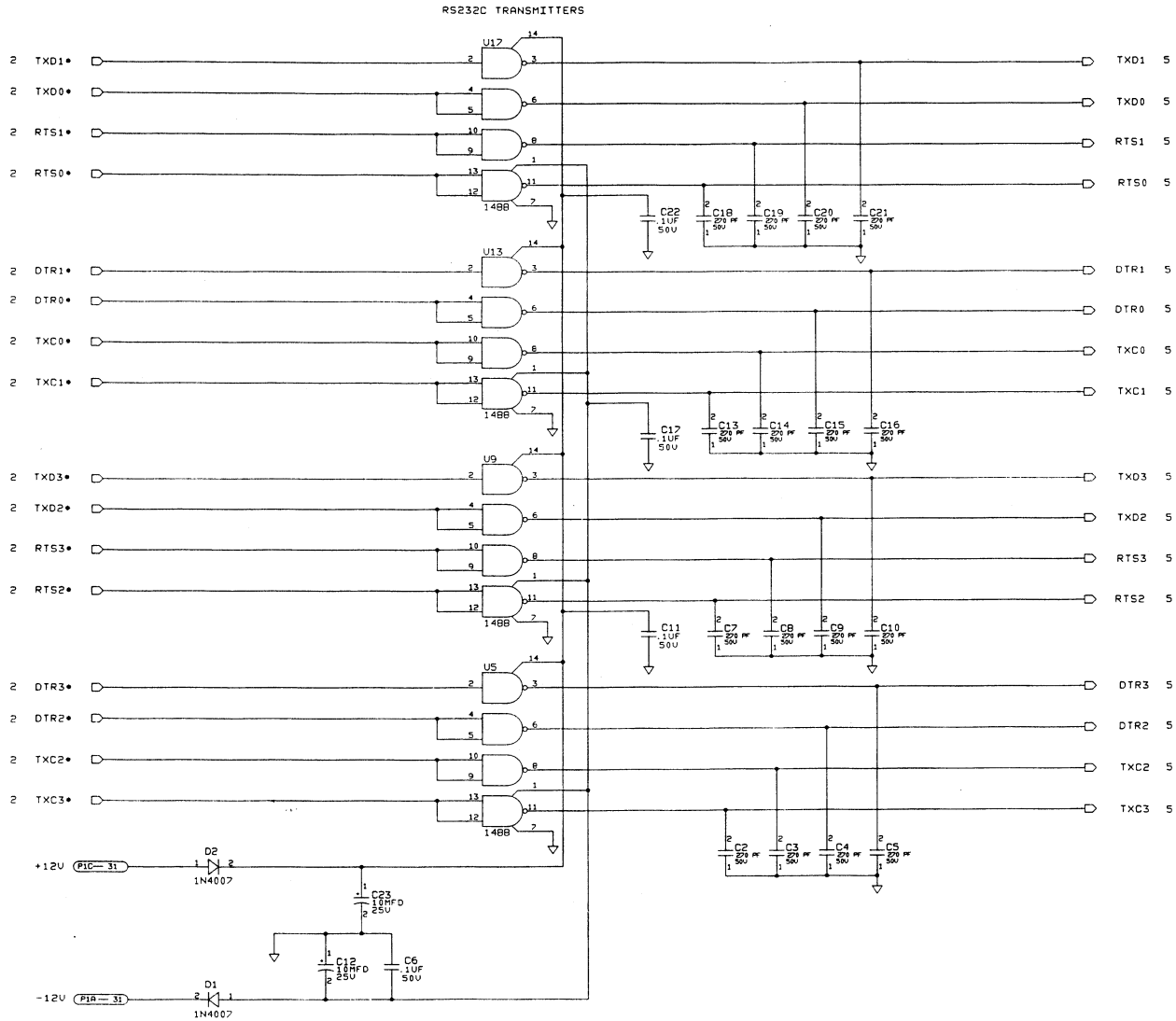
XVME-401 Schematic, Sheet 3 of 4


75172
U16
2 TXD1
2 TXC1*
2 DTR1*
2 RTS1*
IN2
IN3
IN4
IN1
OE
VCC
OUT2
OUT2
OUT3
OUT3
OUT4
OUT4
OUT1
OUT1
OE
GND
J5
+5V
JK2 -1 SD1B
JK2 -2 SD1A
JK2 -28 TT1B
JK2 -21 TT1A
JK2 -16 TR1B
JK2 -17 TR1A
JK2 -7 RS1B
JK2 -8 RS1A
+5V
J2
JK2 -47 +5V
75172
U8
2 TXD3
2 TXC3*
2 DTR3*
2 RTS3*
IN1
IN3
IN4
IN2
OUT1
OUT1
OUT3
OUT3
OUT4
OUT4
OUT2
OUT2
J3
JK2 -26 SD3B
JK2 -27 SD3A
JK2 -45 TT3B
JK2 -46 TT3A
JK2 -41 TR3B
JK2 -42 TR3A
JK2 -32 RS3B
JK2 -33 RS3A
JK2 -25 S61
JK2 -24 SC1
JK2 -50 S63
JK2 -49 SC3
75173
U12
RD1B JK2 - 5
RD1A JK2 - 6
RT1B JK2 - 9
RT1A JK2 - 10
RR1B JK2 - 18
RR1A JK2 - 19
CS1B JK2 - 11
CS1A JK2 - 12
IN3
IN3
IN1
IN1
IN2
IN2
IN4
IN4
OUT3
OUT1
OUT2
OUT4
OE
OE
RXD1 2
RXC1* 2
DCD1* 2
CTS1* 2
75173
U4
RD3B JK2 - 30
RD3A JK2 - 31
RT3B JK2 - 34
RT3A JK2 - 35
RR3B JK2 - 43
RR3A JK2 - 44
CS3B JK2 - 36
CS3A JK2 - 37
IN1
IN1
IN2
IN2
IN4
IN4
IN3
IN3
OUT1
OUT2
OUT4
OUT3
OE
OE
RXD3 2
RXC3* 2
DCD3* 2
CTS3* 2

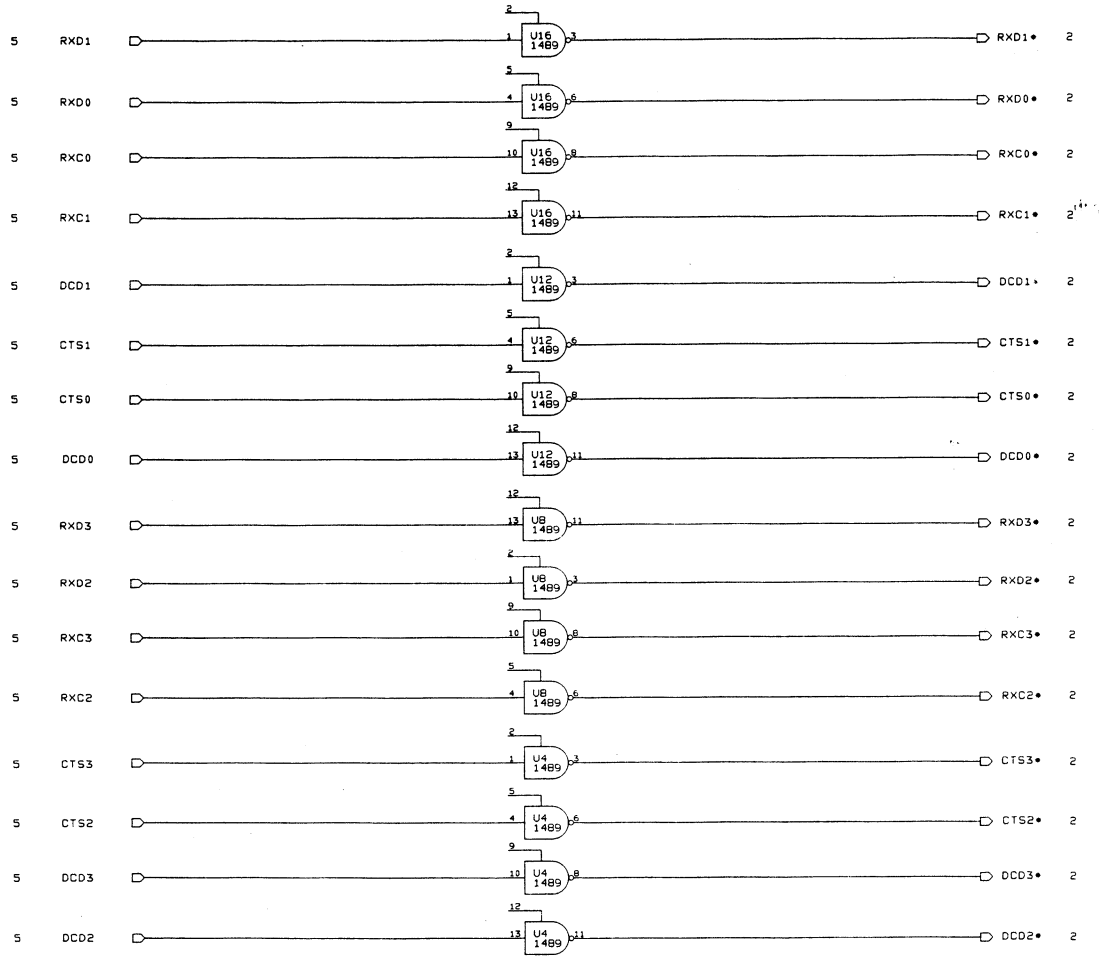


XVME-490 Schematic, Sheet 1 of 5


SERIAL COMMUNICATIONS CONTROLLER #1
SERIAL COMMUNICATIONS CONTROLLER #2
VMEbus DATA BUFFER
LS645 U3
8530 U20
8530 U1
U14 7433
SPARE DEVICES
BD(0:7)
BA(1:3)
RD#
WR#
INTACK#
LWRITE#
BUFFEN#
PCLK
IPEN#
REPEAT=21



XVME-490 Schematic, Sheet 3 of 5

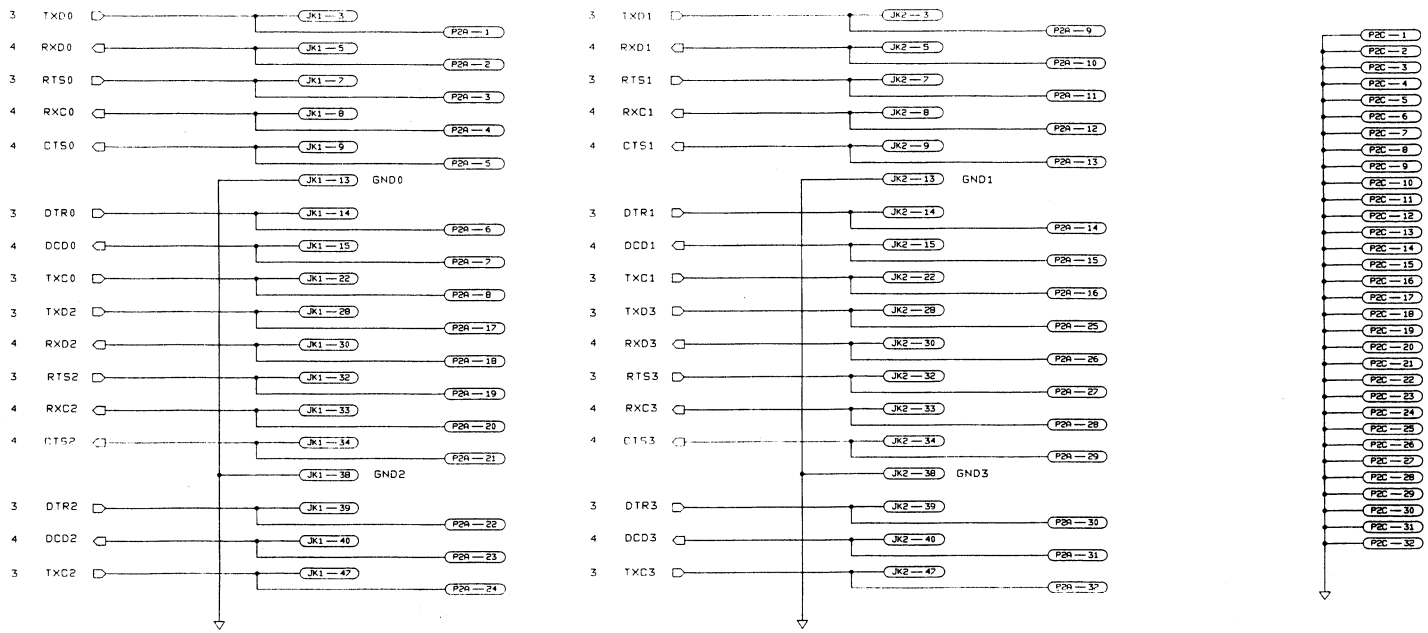


RS232C RECEIVERS

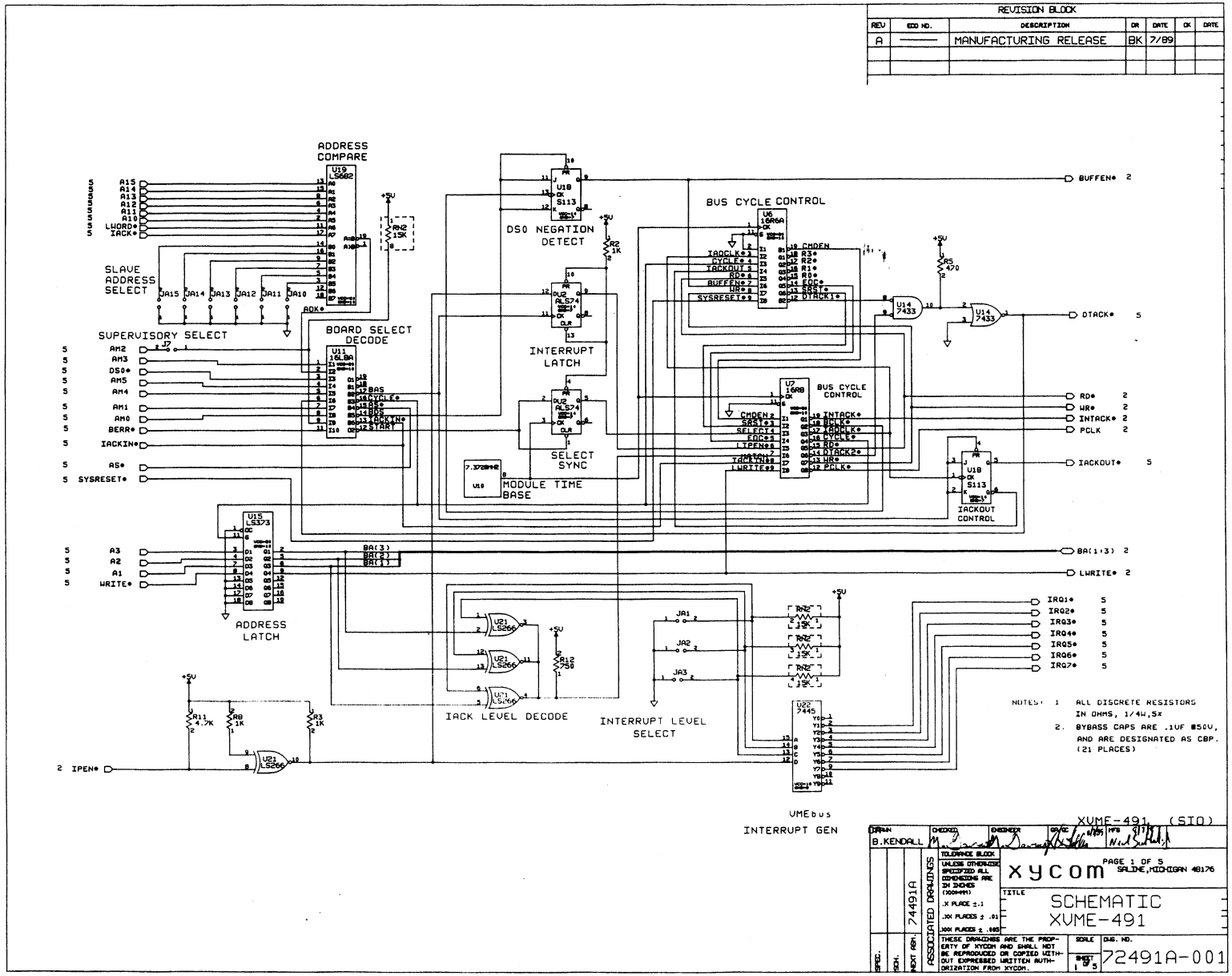
DEVICE	REF. DES.	VCC	GND
1489	U4,8 12,16	14	7
16L8A	U11	20	10
16R8A	U7	20	10
16R6A	U6	20	10
7433	U14	14	7
7445	U22	16	8
74ALS74	U2	14	7
74S113	U18	14	7
74LS266	U21	14	7
74LS373	U15	20	10
74LS645	U3	20	10
74LS682	U19	20	10
8530	U1,20	9	31
7.3728MHZ	U10	14	7

	D2
	P2
	J1
	C46
	R13
	JA15
	RN2
	JK2
JA4-JA9	U22
UNUSED DEVICES	DESIGNATION LAST USED

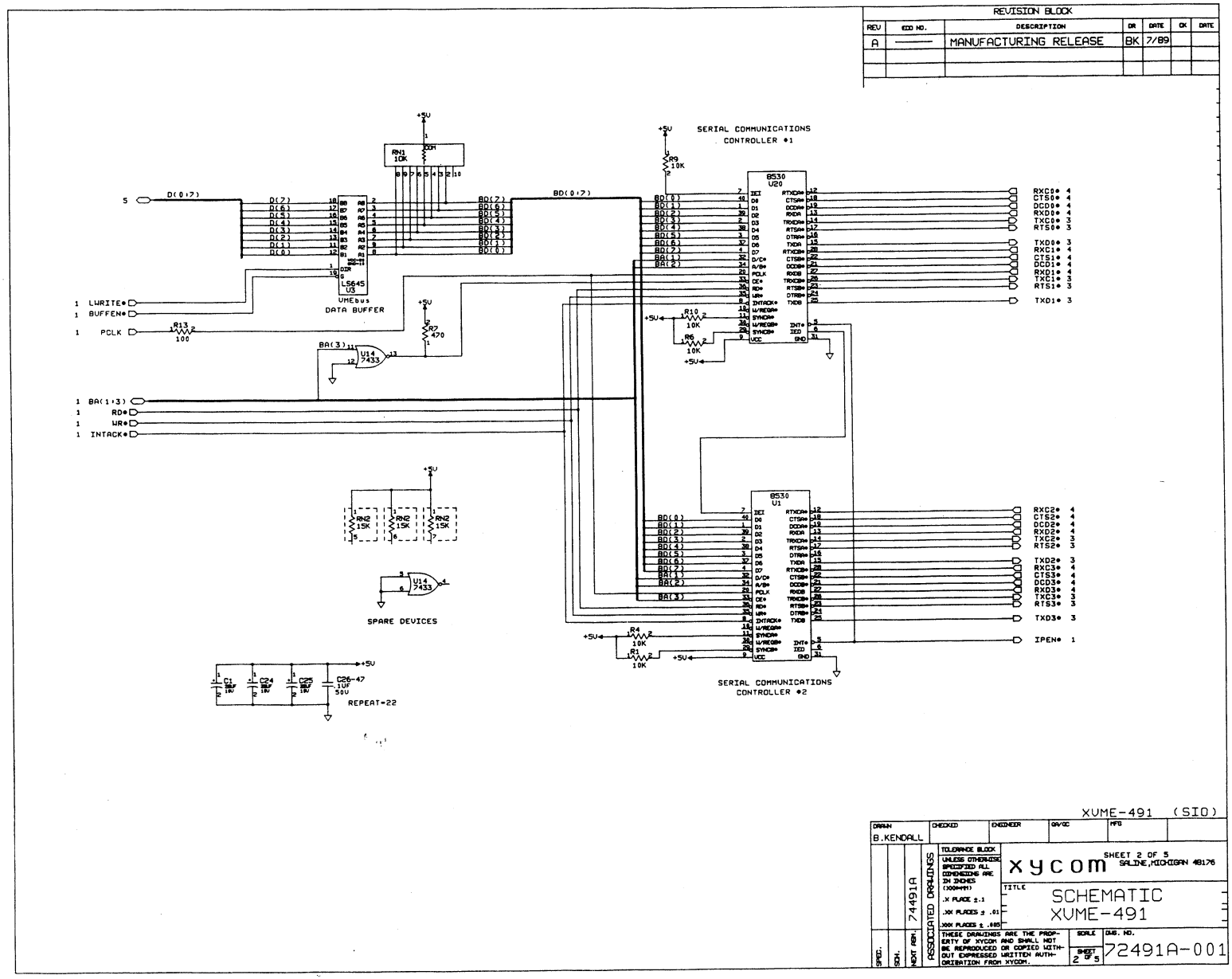
REFERENECE DESIGNATION CHART



XVME-490 Schematic, Sheet 5 of 5



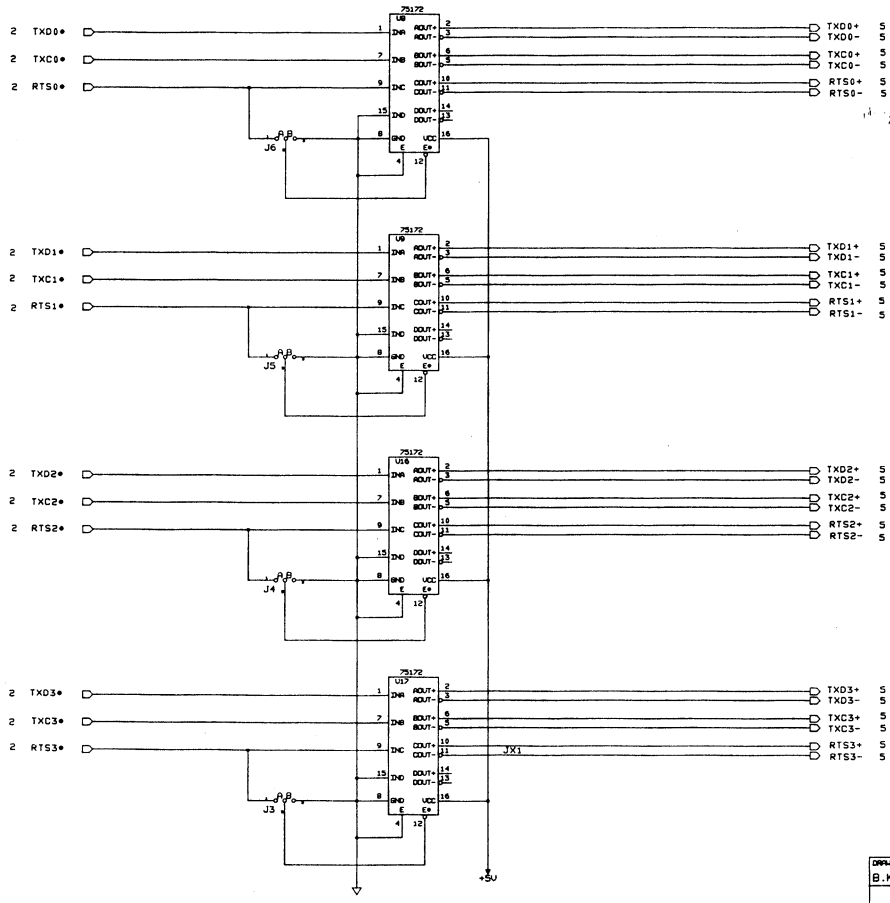
XVME-491 Schematic, Sheet 1 of 5



XVME-491 Schematic, Sheet 2 of 5

REVISION BLOCK						
REV	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
A	———	MANUFACTURING RELEASE	BK	7/89		

DIFFERENTIAL TRANSMITTERS



XVME-491 (SIO)

DRAWN	CHECKED	ENGINEER	QA/QC	MFG
B.KENDALL				

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TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXX=MM)
.X PLACE ± .1
.XX PLACES ± .01
.XXX PLACES ± .005

TITLE
SCHEMATIC
XVME-491

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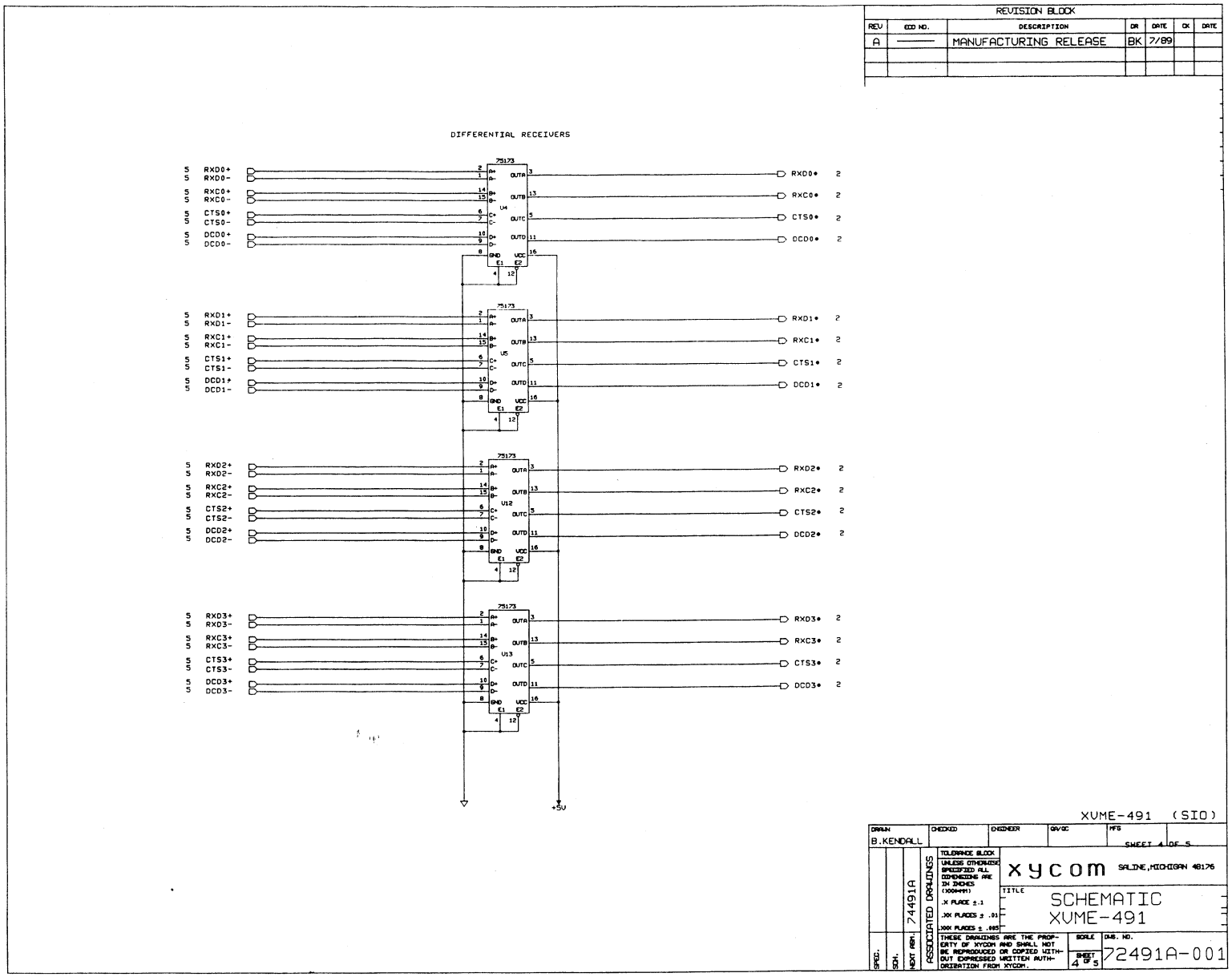
SCALE

DWG. NO. 72491A-001

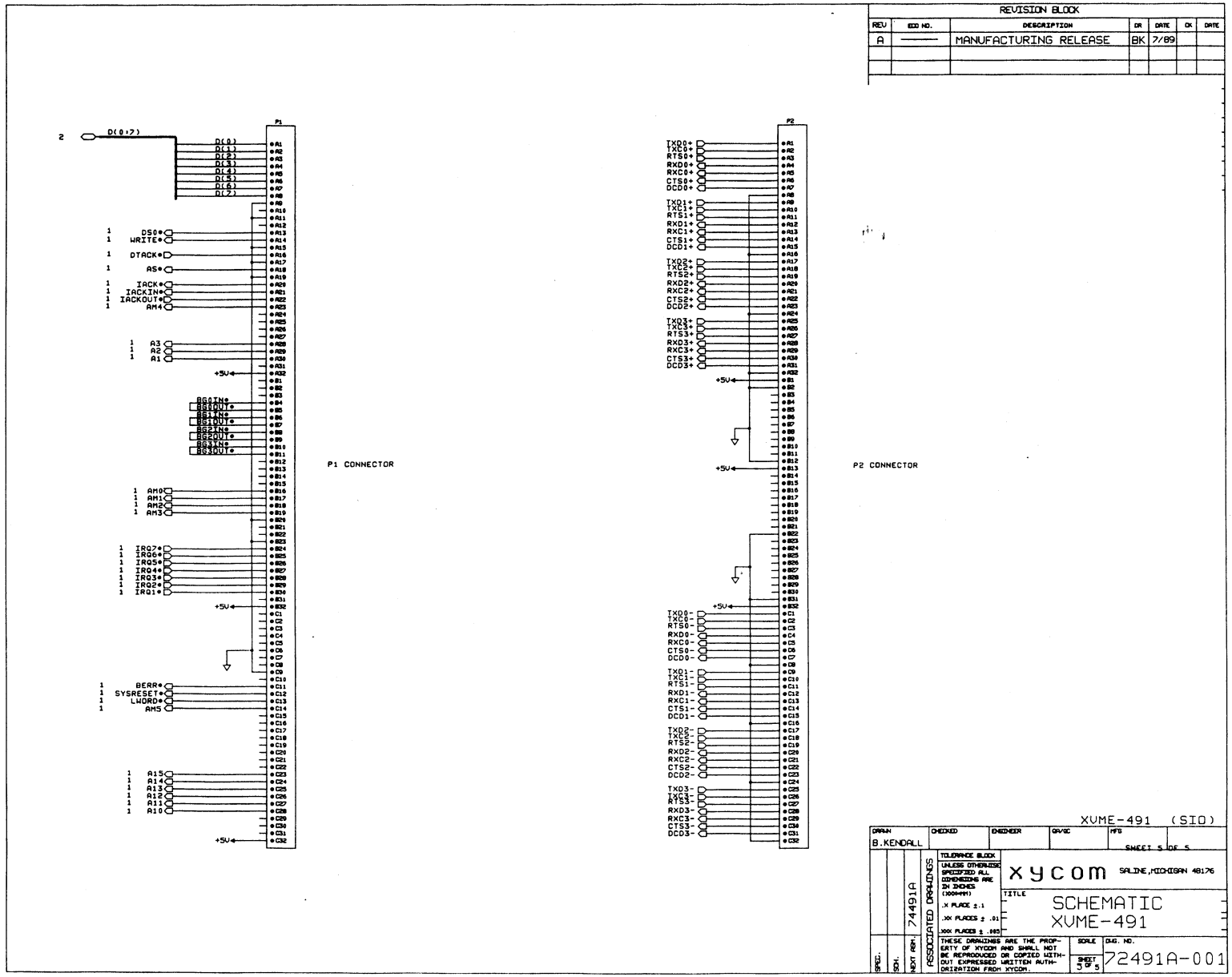
SHEET 3 OF 5

ASSOCIATED DRAWINGS 74491A

SPEC. SCH. NEXT ASY.



XVME-491 Schematic, Sheet 4 of 5


REVISION BLOCK
REV | ECO NO. | DESCRIPTION | DR | DATE | CK | DATE
A | ——— | MANUFACTURING RELEASE | BK | 7/89
P1
P1 CONNECTOR
P2
P2 CONNECTOR
D(0:7)
DS0*
WRITE*
DTACK*
AS*
IACK*
IACKIN*
IACKOUT*
AM4
A3
A2
A1
+5V
BG3IN*
BG3OUT*
BG2IN*
BG2OUT*
BG1IN*
BG1OUT*
BG0IN*
BG0OUT*
AM0
AM1
AM2
AM3
IRQ7*
IRQ6*
IRQ5*
IRQ4*
IRQ3*
IRQ2*
IRQ1*
BERR*
SYSRESET*
LWORD*
AM5
A15
A14
A13
A12
A11
A10
TXD0+
TXC0+
RTS0+
RXD0+
RXC0+
CTS0+
DCD0+
TXD1+
TXC1+
RTS1+
RXD1+
RXC1+
CTS1+
DCD1+
TXD2+
TXC2+
RTS2+
RXD2+
RXC2+
CTS2+
DCD2+
TXD3+
TXC3+
RTS3+
RXD3+
RXC3+
CTS3+
DCD3+
TXD0-
TXC0-
RTS0-
RXD0-
RXC0-
CTS0-
DCD0-
TXD1-
TXC1-
RTS1-
RXD1-
RXC1-
CTS1-
DCD1-
TXD2-
TXC2-
RTS2-
RXD2-
RXC2-
CTS2-
DCD2-
TXD3-
TXC3-
RTS3-
RXD3-
RXC3-
CTS3-
DCD3-
XVME-491 (SIO)
DRAWN B.KENDALL
CHECKED
ENGINEER
QA/QC
MFG
SHEET 5 OF 5
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (MM=MM)
.X PLACE ± .1
.XX PLACES ± .01
.XXX PLACES ± .005
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SPEC.
SCH.
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